

ECE 3714 – Digital Devices and Logic Design

Textbook: Digital Principles and Design, Givone, Donald D., McGraw Hill Publishers, 2003 Edition

I. Binary, Hexadecimal Number Systems

- A. Powers of Two; Powers of Sixteen
- B. Positional Notation
- C. Unsigned Number Representation
 - 1. Range for Fixed Precision
 - 2. Addition/Subtraction with Overflow Determination
- D. Signed Number Representations
 - 1. Signed Magnitude Representation Range for Fixed Precision
 - 2. Ones Complement Representation Range for Fixed Precision
 - 3. Twos Complement
 - a) Range for Twos Complement
 - b) Addition/Subtraction with Overflow Determination
- E. Conversions between Number Systems(Binary, Decimal, Hex)
- F. Sign Extension for Unsigned and Signed Number Representation
- G. Codes
 - 1. Alphanumeric Codes
 - 2. Unit Distance Codes
 - 3. Error Detection Codes (Parity)
 - 4. Simple Error Correction Codes (Hamming)

II. Boolean Algebra

- A. Basic Operations (AND,OR,NOT, NAND, NOR, XOR, XNOR)
 - 1. Truth Tables
 - 2. Logic Symbols
 - 3. Mathematical Equation
- B. Basic Properties and Theorems
 - 1. Idempotent, Involution
 - 2. Commutative, Associative, Distributive
 - 3. Absorption, Consensus, DeMorgan's Theorems
 - 4. Second Distributive Law
- C. Minterm/Maxterm Canonical Formulas
- D. Manipulation of Boolean Formulas
 - 1. Complementation
 - 2. Simplification
 - 3. Shannon's Expansion
 - 4. Sum of Products Form
 - 5. Product of Sums Form
- E. Incomplete Boolean Functions and Don't Care Conditions

III. Physical Gate Properties

- A. TTL Versus CMOS Technologies
- B. CMOS Transistor Diagrams for Basic Gates
- C. Noise Margins
- D. Fan-out
- E. Propagation Delay
- F. Universal Gates
- G. Two-Level AND/OR, OR/AND, NAND/NAND, NOR/NOR Circuits

IV. Simplification of Boolean Expressions

- E. Karnaugh Maps up to Four Variables
- F. Prime Implicants, Implicates
- G. Criteria for Minimality
- H. Multiple Output Minimal Sums

V. Combinational Building Blocks and Programmable Logic Devices

- A. Binary Adders
- B. Comparators
- C. Decoders/Encoders
- D. Multiplexers
- E. Programmable Read Only Memory
- F. Logic Design with Decoders, Multiplexers, PROMS
- G. Programmable Logic Devices (PALs, PLAs)

VI. Altera MaxPlus II Simulation

- A. Graphical Editors
- B. Simulation of Circuits
- C. VHDL Entry of Combinational Networks
- D. Using Jedec Files to Program Devices

VII. Flip Flops and Latches

- A. Bistable Memory Devices
 - 1. SR,D Latch
 - 2. Master-Slave JK and SR FlipFlops
- B. Edge Triggered D FlipFlops
- C. Timing of FlipFlops
 - 1. Propagation Delays
 - 2. Minimum Pulse Width
 - 3. Setup and Hold Times
 - 4. Asynchronous/Synchronous Inputs
- D. Characteristic Equations

VIII. Sequential Building Blocks

- A. Registers
- B. Counters
- C. Shift Registers
- D. Designs and Timing Considerations

IX. Synchronous Sequential Network Models

X. Algorithmic State Machines

- A. ASM Charts
- B. State Assignments using Binary or Gray Codes
- C. Transition Tables
- D. ASM Realizations using Discrete Gates, Multiplexers

XI. Synchronous Sequential Networks Using MaxPlus

- A. Direct ASM to VHDL Equations
- B. ASM Realizations using PLDs