
Computer Aided Digital Systems Design - EE 4743/6743

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Introduction

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Introduction and Contacts

Very Short Bio

- Ph.D., University of Toronto, Canada, 2002
- Thesis: Interacting DES, modeling, verification and supervisory cont.
- 2000-2001: Research Scientist, Rockwell Science Center, CA
- 2002-2007: Research Assistant Professor, Vanderbilt University, TN
- 2007-present: Assistant Professor, ECE Department, MSU

Contact Information

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 - WWW: www.ece.msstate.edu/~sherif
 - Office Hours: MW 1:30-3:00 pm, or by appointment
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Lectures and Labs

Class meeting

- MW 10:00-10:50am, Simrall 102
 - Will have lectures on Fridays also for the first 3-5 weeks to get a fast start on materials
 - Fridays will be mostly used for tests
- Greater class load in the beginning to prepare for lab. More time for labs and project at end of semester

Labs

- Lab session attendance is required to hear TA explanation of lab assignment. Lab at Simrall workstation lab, 1st floor (Simrall 132).
 - Lab assignments due ONE WEEK from your assigned lab time unless otherwise noted
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Requirements and Resources

Prerequisite Topics

- Binary, Octal, and Hexadecimal numbering systems
- Boolean Algebra, Gate level minimization
- Combinational and sequential building blocks. Memory devices
- Synchronous sequential networks (finite state machines

Resources

- Class slides – main source for tests
 - Books:
 - R. Reese, Introduction to Logic Synthesis using Verilog HDL, 2006
 - M. D. Ciletti, Advanced Digital Design With the Verilog HDL, (Optional).
 - Diligent Basys development board
 - Xilinx WebPack software and documentation (Downloadable)
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Course Outline

- **Verilog HDL:** types of Verilog (Structural, Behavioral),
 - **Finite State Machines:** ASM, Verilog implementations, FSM timing
 - **Datapath design:** FMS controller design, memory types and design issues, asynchronous vs. synchronous control
 - **Timing analysis:** computing different delays across the circuit, techniques to increase the clock rate
 - **Scheduling:** design constraints, data flow graph, datapath design, clock and register scheduling, techniques to increase initiation rate
 - **Pipelining:** Requirement analysis, design issues and implementation approach
 - **IO Technologies:** signaling types (applications, technologies, advantages, and disadvantages), eye diagram.
 - **Implementations technologies:** ROMs, PLDs, FPGAs, Gate Arrays, Standard cells, Custom logic.
 - **Design for Test techniques:** Fault analysis
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Course Objectives

By the end of the course, you should learn:

- **Combinational, Sequential, and Structural Verilog HDL.** Write a textual description of a digital schematic which can be compiled and downloaded into a configurable chip.
 - **Implementation Technologies.** Identify target implementations given design guidelines and constraints.
 - **Datapath Design and Control.** Given a datapath, select and design a control mechanism (FSM, Microcode).
 - **System Timing.** Determine worst-case scenarios for timing delays given a specific design.
 - **Testing and Evaluation.** Create a test program to check for opens and shorts in a given design.
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Course Website

- **Current website**

- www.ece.msstate.edu/wiki/index.php/ECE4743_Digital_Systems_Design

- **Resource**

- Syllabus
- Course updates
- Tutorials
- Lecture notes, supplemental readings
- Previous homework assignments
- Project information
- Sample tests and homework

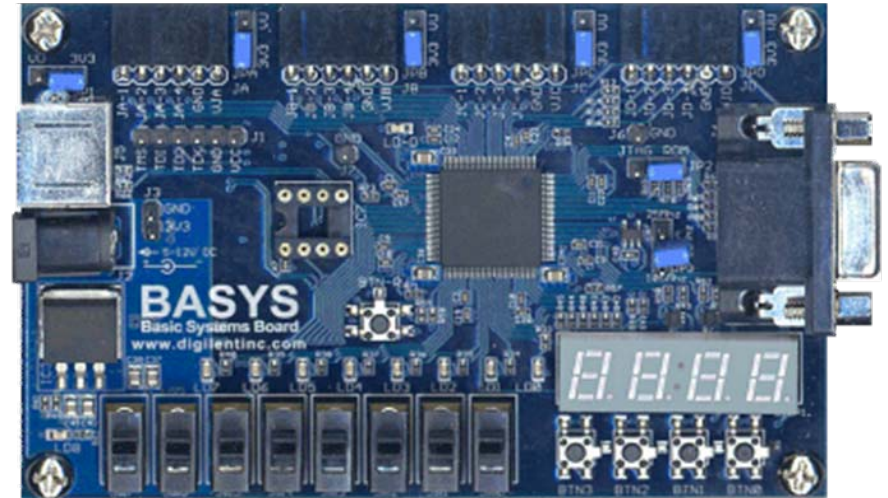
- **Check it often**

Course Software

- We will be using a package called Xilinx ISE WebPack for digital logic programming. Can be downloaded from the Xilinx webpage
 - Software is the same as used by practicing engineers in industry
 - We will discuss how to install and use the software in lab.
 - The labs will be oriented around your laptops, so you will need to install the software yourself.
 - You must have the software downloaded before coming to lab since it is a very large download (~850MB). Instructions for downloading it are included in lab 1.
 - This software is also available on the workstations in the lab if you do not have a laptop.
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Course Hardware

- Purchase development board
 - Digilent Basys board,
 - Can be purchased directly from Digilent Inc. homepage (\$59).
- Each board has 8 LEDs, 8 switches, 4 push buttons, and a 4 digit numerical display.
- There are also connections for a VGA monitor and a PS/2 port for keyboards/mice.
- Reference manual and board schematic are available to download
- Strongly recommending doing the labs on your laptops
- If you don't have a suitable laptop, some computers will be available in lab for development and programming



Class Projects

- Team project this semester lasting 3-4 weeks
 - Uses the Basys development board interfaced with inputs and output devices
 - Potential project topics will be posted later
 - During the semester you will submit a proposal for your project
 - Must be approved by the instructor
 - The project must have a high relevance factor and be attractive
 - Several milestones
 - Forming teams
 - Project status reports
 - Project demonstrations
 - Project final report
 - More details coming later in the course
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Attendance

- Not taking attendance for classes
 - Expected for tests and finals
 - NO make-up tests
 - possible exceptions for extreme cases
 - Tests based on in-class discussion
 - STRONGLY RECOMMEND coming to class
 - Ask QUESTIONS during CLASS to SLOW things down
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Grading and Tests

Grad distribution

- Tests (5): 40%
- Final: 30%
- Lab: 20%
- Project: 10%

Grade levels

A	100-90
B	89-80
C	79-70
D	69-60
F	59-0

Tests

- You must achieve at least a 60% grade average on ALL in-class material (exams+ lab+ project) to pass the course.
 - There will be five tests (in addition to the final and lab test). Your lowest test grade will be dropped
 - Previous tests are posted on the course website.
 - Test dates will be announced at class least one week in advance
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Test Re-grade policy

- You may request one re-grade for each exam
 - In writing justify the change
 - Even for small errors
 - Submit your exam and your statement
 - To me personally, or under my door, or in my mailbox
 - However, I cannot guarantee that I will receive the submission unless it is given to me personally.
 - Must be submitted within one week of the date the exams are returned
 - I will consider each case and return my response in writing along with your exam
 - Once I have given my response, I will not discuss the matter further
 - Make sure you say everything you want to in your first submission
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On Upper Level Courses

- This is an upper-level course (Jr/Sr/Graduate). This means that you will soon graduate and enter industry
 - In upper level courses, topics are discussed in less details compared with lower level course
 - Students are expected to show some self-motivation, look up information, ask questions, etc. on all of the class topics
 - If you do not understand a topic, ask questions of the professor, your peers, and seek outside knowledge sources. This is what will be expected of YOU in industry
 - It can be a difficult transition in going from the previous instruction style to this instruction style - the first step is to recognize YOUR RESPONSIBILITIES
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Student Responsibilities

- Ask questions! BE CURIOUS!!!! This is one of the most important aspects of an engineer - if you are not curious, then do not be an engineer. If you are simply after money, be an investment broker, speculate in real estate, win a lottery, etc.
 - Investigate alternate data sources other than the professor and the TA.
 - Understand the relevance of what you are being asked to learn - after all, you will be expected to perform as a real engineer in a short period of time and you need to understand how to apply this knowledge!
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Academic Dishonesty

- DISCUSS work verbally
 - Talk about methods/procedures
 - NOT results
- Do not SHOW work
- Do not COPY work
- This includes schematics, VHDL code, simulation files, etc.
- Both parties are guilty
 - Showing work is just as bad as copying work
- Will result in an XF or a permanent F in your record
 - For graduate students – D or F = expulsion
- No team assignments for labs
- See <http://students.msstate.edu/honorcode/>

MSU Honor Code

“As a Mississippi State University Student I will conduct myself with honor and integrity at all times. I will not lie, cheat, or steal, nor will I accept the actions of those who do”