Computer Aided Digital Systems Design - EE 4743/6743

Sherif Abdelwahed

Final Review

Department of Electrical and Computer Engineering
Mississippi State University

Project Matters Notes

- Final project phase is due now. Include:
  - Final top-level schematic
  - Verification plan
  - Deliverables and outputs
  - Project updates
  - Project snapshots
  - Project files (source code).
- Project demo,
  - Friday April 25th.
  - 3:00pm – 5:00pm in DSD lab (Simrall 132).

Project Demo – 30 minutes

- Describe the function of your design and how it is implemented
- Show that your design works correctly for all operations.
- Describe any optimizations you made to your design
- Describe how you tested your design
- Describe any known problems with your design
- Present area, delay, and latency results for your final design
- Describe the contributions of each team member to the project
- Answer questions related to your design
- All team members should be participate unless excused

Final Exam

- Final Exam:
  - Monday, April 28th
  - 8:00 am-11:00 am in Simrall 102.
- Target: Everything in course
  - Class Slides
  - Labs
- Test is closed book
  - No computer (no Verilog simulator or tools, etc.)
  - Cell phones should be turned off during the exam
- You are allowed one page (two sides) of notes
- Problems at same level as the previous tests
- Example tests available online

Strategy and Scope

- Review all lectures and class notes
- Look over old homework and tests
- Check the tests of this year:
  - See where you made mistakes
  - Estimate similar questions
- Prepare a good set of notes
- The following review classes will not be targeted in the final test:
  - Combinational logic review
  - Sequential logic review
  - FSM review
- However, these materials are used indirectly throughout the course

Verilog HDL

- Verilog coding styles
  - Structural, RTL, Behavioral
- Implementation types
  - Combinational, sequential, and FSM
- Syntax and semantics
  - Data types, constants
  - Statements (concurrent vs. sequential),
  - Assignments (blocking vs. non-blocking).
  - Procedural blocks (always, initial)
  - Control and loops
- Basic building blocks
  - Combinational: Adders, mux, …
  - Sequential: Counters, FF, shift registers, …

Verilog HDL

- Finite State Machine design
  - Moore vs. Mealy, and how they are coded
  - Use of parameters to define state values
  - State encoding
  - ASM
  - Verilog implementations: , 2, or 3 process implementation
  - FSM timing
- Review questions:
  - Given a Verilog code, create the corresponding ASM
  - Write the code for basic design blocks with different configurations:
    - Ex: shift reg. with sync. load, counter with async. reset.
  - Structural design from building blocks using parametrized instantiation.

Implementations Technologies

- ASIC technologies
  - Full Custom, Standard Cell, Gate Array
- Programmable technologies
  - Programmable Logic Devices (PLDs)
  - Complex PLDs (CPLDs)
  - Field Programmable Gate Arrays (FPGAs)
- Differences between related technologies
- Advantages and disadvantages of different technologies
- FPGA Internals
  - Main building blocks (LUT, RAM, etc.)
  - IO structure
- Programmability options

Datapath Design

- FMS controller design
- Memory types and design issues
- Async. v.s. sync control
- Datapath design examples
- Review questions:
  - Given a datapath/controller design and timing diagram draw the corresponding ASM diagram
  - Given a datapath planning draw the corresponding design and show all the control signals

System Timing

- Setup and hold times
- Computing different delays across the circuit
- Longest paths in sequential systems
- Chip to chip timing calculation
- Techniques to increase the clock rate
- Review questions
  - Given a circuit with known gate and FF propagation delays, compute the different delays accross the circuit
  - Compute the clock period
  - Extend the timing analysis for registered inputs/outputs
  - Extend the timing analysis for chip to chip

Scheduling

- Design constraints
- Date flow graph
- Datapath design for given resource and timing constraints
- Clock and register scheduling
- Techniques to increase initiation rate
- Review Questions
  - Given a data flow graph
    - Estimate the minimum number of execution units required
    - Create the operation schedule
    - Perform register scheduling and register assignment

Design for Test techniques

- Types of faults
- Fault analysis: detectability, sensitization, etc.
- Fault coverage
- Fault simulation
- Automated Test Vector Generation
- Design for testability
- Built-In Self Test (BIST) Approach
- Scan Path Design
- IEEE 1149.1 (JTAG)
- Review question:
  - Find a test vector for a given stuck at fault in a circuit
  - Check if a fault is detectable by a given test vector

More Topics

- VGA, LFSR, and PWM
- Pipelining
  - Requirement analysis
  - Design issues and implementation approach
- IO Technologies
  - Signaling types: their applications, technologies, advantages, and disadvantages.
  - Eye diagram
  - Synchronous and source synchronous signaling.