

EE 4743/6743- FALL 2007  
COMPUTER AIDED DESIGN OF DIGITAL SYSTEMS  
PREREQUISITE TOPICS

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NUMBER SYSTEMS

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- Binary, Octal, and Hexadecimal numbering systems.
  - Signed and unsigned number Representations. 1s and 2s complements.
  - Conversion between number systems Binary to Decimal – Positional Notation
  - Addition and Subtraction of Binary and Hex numbers. Operation overflow.
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BOOLEAN ALGEBRA

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- Boolean Operations: AND, OR, NOT, NAND, NOR, XOR, XNOR (truth tables, logic symbol, equation symbol).
  - Basic theorems and properties:
    - Commutative, Associative, and Distributive laws
    - Duality – replace ANDs with OR, OR with AND, 1 with 0, 0 with 1
    - DeMorgan's Laws; Proof of theorem by truth table
  - Minterms, Maxterms, Canonical forms of equations given truth table.
  - SOP (sum of products) and POS (product of sums) forms, their implantations and transformation.
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IMPLEMENTATION OF LOGIC

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- Transistors, voltage levels, propagation delay ( $T_{phl}$ ,  $T_{plh}$ ), and delay path
  - Complete logic families; 7400 devices
  - PLDs (programmable logic device):
    - PALs (programmable ANDs, fixed Ors),
    - PLAs (Programmable ANDs, Programmable ORs)
    - PROMs (fixed ANDs, Programmable ORs)
  - Memories.
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GATE-LEVEL MINIMIZATION

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- Prime implicants; Essential prime implicants; Non-essential prime implicants
  - Incompletely Specified Functions (don't cares)
  - The map method
  - Writing minimum SOP equations, POS equations
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COMBINATIONAL BUILDING BLOCKS

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- Decoders: functional description, circuit diagram, realization of expressions to minimize the total number of input terminals
- Multiplexers: AND/OR implementation, general equation, Circuit Diagram, Realization of expressions, Multiplexer trees
- Adders: Half Adder, Full Adder Circuit Diagrams, Cascaded Iterative Networks

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## BISTABLE MEMORY DEVICES

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- Latches (State Tables, Characteristic Equation):
  - SR Latch (NOR Implementation),
  - S'R' Latch (NAND Implementation),
  - R Dominant, S Dominant SR Latches,
  - D Latch, Gated D Latch
- FlipFlops (State Tables, Characteristic Equation):
  - Pulse- and edge-triggered FF,
  - MS, D, JK, and T FlipFlops
- Timing for FlipFlops, Latches:
  - Positive/Negative edge triggering,
  - Period/Frequency relationship,
  - Pulse width and duty cycle,
  - Synchronous/ Asynchronous inputs, Propagation delays for synchronous Inputs, Asynchronous inputs setup/hold times and characteristic equations

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## SEQUENTIAL BUILDING BLOCKS

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- Registers.
- Shift Registers
- Counters.
- Ripple counters.
- Synchronous binary counters

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## SYNCHRONOUS SEQUENTIAL NETWORKS (FINITE STATE MACHINES)

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- General Model. Structure of a Clocked Synchronous Sequential Network
- Moore/Mealy Machine Models
- Writing next state and output equations from a diagram (analysis)
- Bubble Diagrams and ASM Charts
- Design of Clocked Synchronous Sequential Networks
- Realizations using individual gates and FF or PLDS
- Timing of synchronous sequential networks