

EE 4743/6743- FALL 2007  
COMPUTER AIDED DESIGN OF DIGITAL SYSTEMS  
CLASS POLICY AND SYLLABUS

---

---

CONTACT INFORMATION

---

**Professor:** Sherif Abdelwahed

**Office:** Simrall 333

**Phone:** 325-6903

**E-mail:** sherif@ece.msstate.edu

**Web page:** <http://www.ece.msstate.edu/classes/ece4743/fall2007/index.html>

**Office Hours:** Simrall 333, MW 1:30-3:00 pm, or by appointment.

---

PREREQUISITES AND RESOURCES

---

**Prerequisites:** ECE3714 Digital Devices

**Resources:**

- Course Notes
  - Book: Introduction to Logic Synthesis using Verilog HDL, by Robert B. Reese (optional).
  - Xilinx Foundation software (Xilinx ISE WebPACK – available for free download).
  - Digilent Basys development board (available from Digilent Inc. web site for 59\$).
- 

COURSE OBJECTIVES

---

By the end of the course, you should be able to do:

- **Combinational, Sequential, and Structural Verilog HDL.** Write a textual description of a digital schematic which can be compiled and downloaded into a configurable chip. Designs can be used modularly to minimize design time and maximum reusability.
  - **Implementation Technologies.** Identify target implementations given design guidelines and constraints. Determine which design tool is most appropriate to use for a given design (VHDL, Verilog, Schematic Capture).
  - **Datapath Design and Control.** Given a datapath, select and design a control mechanism (FSM, Microcode). Given an equation or process, design a dataflow graph. Then design a datapath following the constraints of the system.
  - **System Timing.** Determine worst-case scenarios for timing delays given a specific design. Minimize the worst-case using good design techniques (pipelining, scheduling, registering I/O).
  - **Testing and Evaluation.** Create a test program to check for opens and shorts in a given design.
- 

GRADING

---

Final letter grades are assigned based on the class distribution. Student grades-to-date will be emailed periodically. It is your responsibility to verify that your grades have been correctly entered. In addition to the percentage distributions below, you must achieve at least a 60% grade average on ALL in-class material (exams + lab) in order to get a "D" in the course. This prevents you from simply ignoring either the in-class material or out-of-class material in favor of the other.

<b>Grade distribution</b>	
Tests	45%
Final	25%
Labs	20%
Project	10%
Total:	100%

<b>Grade levels</b>	
A	100-90
B	89-80
C	79-70
D	69-60
F	59-0

---

## TESTS

---

There will be five tests including the final. Test date will be announced at least two weeks in advance except for the first take home test. Your lowest test grade will be dropped. Your test average will be computed from the three highest test grades.

**Test re-grade policy:** If you think there has been an error in grading your exam, you may request one re-grade for each exam. The request must be in writing and contain your entire argument justifying the change. Submit your exam and your statement either to me personally, or put it under my door, or put it in my mailbox. However, I cannot guarantee that I will receive the submission unless it is given to me personally. (You may submit it under the wrong door or mailbox, for example) It must be submitted within one week of the date the exams are returned. I will consider each case and return my response in writing along with your exam. Once I have given my response, I will not discuss the matter further. Make sure you say everything you want to in your first submission.

---

## LAB

---

The workstation lab on the first floor of Simrall is considered an OPEN lab. This means you can work on your assignment anytime the lab is open and you can find a free machine. Your assigned lab period is a time in which you will be GUARANTEED a machine; you should go to the lab during your assigned lab period because the lab assistant will be available for questions and help. Labs are due one week after it is assigned. You should start on the lab IMMEDIATELY since the assignment will generally take longer than the assigned lab period.

---

## PROJECT

---

There will be a team project this semester lasting three weeks. The project will use the Basys development board. Suggestions for projects will be provided. During the semester the students will submit a proposal for their project, and it must be approved by the instructor. The project must have a high "wow" factor and be attractive.

---

## ATTENDANCE

---

Students are expected to be present for all tests and for the final exam. In extreme cases, I may arrange a make-up test. I will not be taking regular attendance, but I strongly suggest coming to class as the tests are based off material discussed in class. It is the student's responsibility to contact me IN ADVANCE to explain the situation and arrange a makeup.

---

## ACADEMIC DISHONESTY

---

You may **DISCUSS** work, and **verbally** answer questions about lab work from other students. You may NOT **SHOW** your work to another student, or provide an 'old copy' as an example. Looking at or copying any material (schematics, VHDL files, simulation files, etc.) from another student is considered academic dishonesty. The person providing this material would also be guilty of academic dishonesty. If I find a student guilty of academic dishonesty, expect an **F** in the course and an academic dishonesty claim to go into your permanent academic record. For graduate students, an **F** in any course results in immediate expulsion. For more information on the school honor code see <http://students.msstate.edu/honorcode/>