

Generalized Cube Networks for Implementing Dynamic Element Matching Digital-to-Analog Converters

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Abstract

Dynamic element matching (DEM) has been used to increase the spurious free dynamic range of digital to analog converters (DACs). In this paper, two DEM networks, the Full Randomization DEM (FRDEM) network and the binary tree (BT) network, are shown to be equivalent to an appropriately connected generalized cube network (GCN). A comparison of these two networks and the GCN shows that the BT network has the lowest hardware complexity for two to six bit DACs and that the FRDEM network has the lowest hardware complexity for DACs with seven bits or more.

1. Introduction

Dynamic element matching (DEM) is a dynamic process that can reduce the effects of component mismatches in electronic circuits. DEM techniques dynamically rearrange the interconnections of mismatched components so that the time averages of the equivalent components at each of the component positions are nearly equal. Some digital-to-analog converters (DACs) use DEM to reduce harmonic distortion caused by mismatched elements [1]-[2]. In this paper, the *Full Randomization* dynamic element matching (FRDEM) network [3] and the binary tree (BT) network [4] are shown to be equivalent to an appropriately connected generalized cube network (GCN). A comparison of the hardware complexity of the FRDEM network, the BT network and its equivalent GCN shows that the BT network has the lowest hardware complexity for two to six bit DACs and that the FRDEM network has the lowest hardware complexity for DACs with seven bits or more.

2. Dynamic element matching DAC architectures

An ideal DAC transforms a B -bit digital signal, $x(n)$, into an analog signal, $y(t)$, such that $y(nT) = ax(n)$, where a is a constant, T is the DAC's sampling period and n is an integer that indexes the sequence x . In practice, DACs contain mismatched circuit components that cause con-

version errors in the analog output signal, $y(t)$, such that $y(nT) = ax(n)+e(n)$ where $e(n)$ is a sequence representing DAC conversion errors. A significant portion of $e(n)$ contains the DAC's harmonic distortion that reduces the DAC's spurious free dynamic range (SFDR). Thus, a DAC's harmonic distortion can be reduced and its SFDR increased by decreasing component mismatch errors in the DAC circuitry.

Some DAC designs reduce component mismatches by using special fabrication processes or by laser trimming components; however, component mismatches cannot be completely eliminated. As an alternative to special fabrication processes, DEM reduces the effects of component mismatches by varying the components' interconnections. If the interconnections can be varied such that the mismatched components' virtual positions are fully randomized, the harmonic distortion caused by the mismatched components is transformed into white noise [2]. Therefore, DEM can decrease a DAC's harmonic distortion and increase its SFDR at the expense of reducing the DAC's signal to noise ratio (SNR).

2.1. A stochastic dynamic element matching DAC topology

Figure 1 shows a B bit stochastic DEM DAC topology that performs DEM by mapping a B bit input signal, $x(n)$, to 2^B single bit DACs through a 2^B line stochastic network [1]. In this topology, a thermometer coder converts the B bit binary coded signal, $x(n)$, into a 2^B bit thermometer coded signal, $t(n)$. Without the stochastic network, the thermometer coded signal, $t(n)$, activates the lower $x(n)$ single bit DACs. Ideally, each deactivated single bit DAC generates an analog signal of amplitude zero, and each activated single bit DAC generates an analog signal of amplitude a . The outputs of all the single bit DACs are summed to produce the DAC's output $y(nT)$.

In practice, mismatched components between each of the single bit DACs cause deterministic conversion errors that cause harmonic distortion and reduce the DAC's SFDR. By randomizing the mapping between the thermometer coded signal, $t(n)$, and the single bit DACs, the positions of mismatched DACs can be virtually altered.

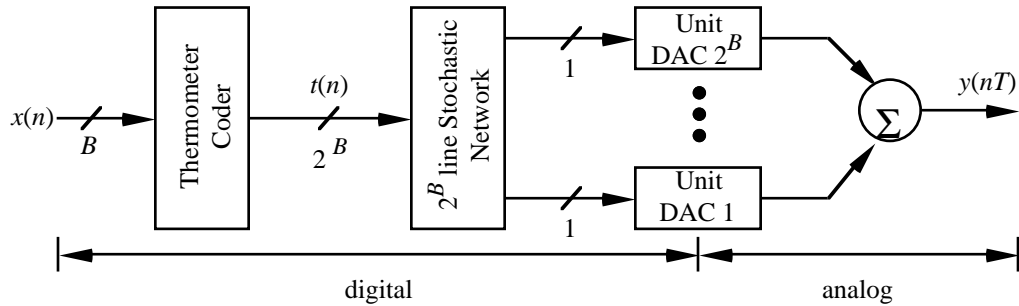


Figure 1. General topology of a B bit stochastic DEM DAC.

As a result of the virtual rearrangement of components, the harmonic distortion is transformed into a white noise signal. Therefore, using DEM, a DAC's harmonic distortion can be decreased and its SFDR range increased at the expense of decreasing the DAC's SNR.

2.2. Full randomization dynamic element matching network

In [3], the thermometer coder and the 2^B line stochastic network shown in Figure 1 were implemented using a single multistage interconnection network named the *Full Randomization* dynamic element matching (FRDEM) network. Figure 2 shows the fundamental switching block, $S_{k,r}$, used to construct FRDEM networks. The switching block's input, $b(n)$, is a $k+1$ bit signal. When the control signal, $c_{k-1}(n)$, is a logical zero, $S_{k,r}$ sends $b(n)$'s k LSBs to the lower outputs and k copies of $b(n)$'s MSB to the upper outputs. When the control signal, $c_{k-1}(n)$, is a logical one, these outputs are exchanged, i.e. $S_{k,r}$ sends $b(n)$'s k LSBs to the upper outputs and k copies of $b(n)$'s MSB to the lower outputs. The switching block, $S_{0,1}$, shown in Figure 3 is a one bit FRDEM network. In general, a $k+1$

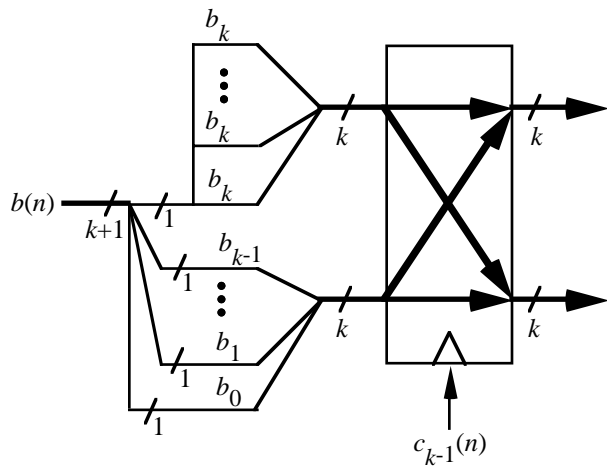


Figure 2. Switching block, $S_{k,r}$, for the FRDEM network.

bit FRDEM network can be constructed by connecting two k bit FRDEM networks with the switching block, $S_{k,1}$ as shown in Figure 4.

To use a B bit FRDEM network in a B bit stochastic DAC, append a logical zero to the LSB of the B bit input signal, $x(n)$, and input this $B+1$ bit signal into a B bit FRDEM network. The FRDEM network outputs are input to 2^B unit DACs as shown in Figure 1. If the FRDEM network's control signals, $c_k(n)$ for $k=0, 1, \dots, B-1$, are random bit sequences, the input signal, $x(n)$, activates $x(n)$ unit DACs randomly each sample [3].

2.3. Binary tree dynamic element matching network

In [4], the thermometer coder and the 2^B line stochastic network shown in Figure 1 were implemented using a binary tree (BT) network. Figure 5 shows a one bit BT network. In general, a $k+1$ bit BT network can be constructed by connecting two k bit BT networks as shown in Figure 6. When the control signal, $c_k(n)$, is a logical zero, the network sends 2^k copies of $b(n)$'s MSB to the upper outputs and $b(n)$'s k LSBs to the lower k bit BT network which generates 2^k outputs from these LSBs. When the control signal, $c_k(n)$, is a logical one, these outputs are exchanged. The BT network's high impedance output can be pulled to an appropriate logic level by external cir-

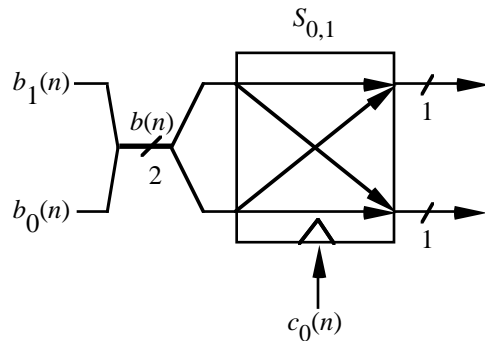


Figure 3. A one bit FRDEM network.

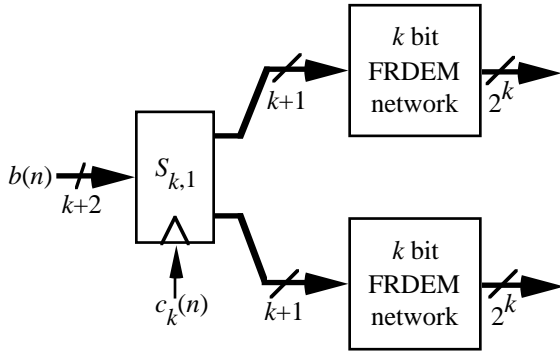


Figure 4. A $k+1$ bit FRDEM network.

cuitry.

To use a B bit BT network in a B bit stochastic DAC, input the B bit input signal, $x(n)$, into a B bit BT network. The BT network's single high impedance output is pulled to a logical zero. These outputs are input to 2^B unit DACs as shown in Figure 1. If the BT network's control signals, $c_k(n)$ for $k = 0, 1, \dots, B-1$, are random bit sequences, the input signal, $x(n)$, activates $x(n)$ unit DACs randomly each sample [4].

2.4. Generalized cube implementations of the FRDEM and binary tree networks

An appropriately connected B bit generalized cube network (GCN) can be configured so that it is equivalent to the FRDEM network and the BT network.

Theorem: The n bit FRDEM network is equivalent to an n bit GCN.

Proof (by induction): The switching block, $S_{0,1}$, shown in Figure 3, is a one bit FRDEM network and is equivalent to a one bit GCN. To illustrate, when $c_0(n)$ is a logical zero, both networks route $b_1(n)$ to the upper output and $b_0(n)$ to the lower output. When $c_0(n)$ is a logical one, both networks exchange these outputs.

Assume that the k bit FRDEM network and the k bit GCN are equivalent. The $k+1$ bit FRDEM network can be partitioned into two k bit FRDEM networks connected by switching block, $S_{k,1}$, as shown in Figure 4. Switching

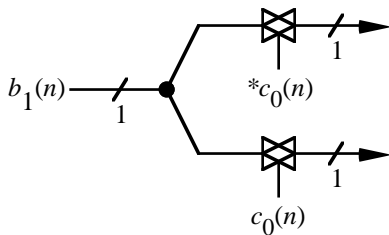


Figure 5. One bit BT network.

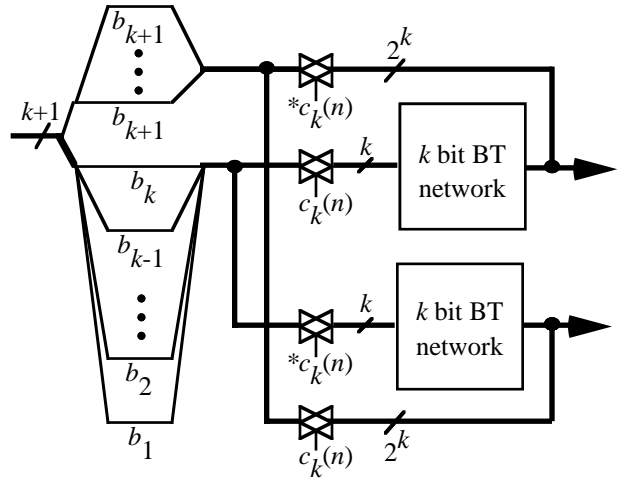


Figure 6. A $k+1$ bit BT network.

block, $S_{k,1}$, performs the cube _{k} operation. As shown in Figure 7, the $k+1$ bit GCN can be partitioned into two k bit GCNs by setting all of the most significant stage interchange switches to operate in unison. When operated in this manner, the first stage of a GCN performs the cube _{k} operation [5]. Thus by induction, the n bit FRDEM network and n bit GCN are equivalent for $n \geq 1$. ■

Theorem: The n bit FRDEM network is equivalent to an n bit BT network when the BT network's high impedance output is set to the LSB of the FRDEM network's input.

Proof (by induction): The switching block, $S_{0,1}$, shown in Figure 3, is a one bit FRDEM network and is equivalent to the one bit BT network shown in Figure 5 when the BT network's high impedance output is set to the LSB of the FRDEM network's input. To illustrate, when $c_0(n)$ is a logical zero, both networks route $b_1(n)$ to the upper output, the FRDEM network routes $b_0(n)$ to the lower output and the BT network generates a high impedance node, which is set to $b_0(n)$, at the lower output. Similarly, when $c_0(n)$ is a logical one, both networks exchange these outputs.

Assume that the k bit FRDEM network and the k bit BT networks are equivalent when the BT network's high impedance output is set to the LSB of the FRDEM network's input. The $k+1$ bit FRDEM network can be partitioned into two k bit FRDEM networks connected by switching block, $S_{k,1}$, as shown in Figure 4. If the control signal, $c_k(n)$, is a logical zero, the input to the upper k bit FRDEM network is k copies of the MSB of $b(n)$, and the input to the lower k bit FRDEM network is the k LSBs of $b(n)$. Therefore, when $c_k(n)$, is low, the upper k bit FRDEM network outputs 2^k copies of the MSB and the lower FRDEM network generates 2^k outputs from the

LSBs. Similarly, these outputs are exchanged when $c_k(n)$ is a logical one. As illustrated by Figure 6, the $k+1$ bit BT network functions identically. Therefore by induction, the n bit FRDEM and the n bit BT networks are equivalent for $n \geq 1$ when the BT network's high impedance output is set to the LSB of the FRDEM network's input. ■

Corollary: The n bit GCN and the n bit BT network are equivalent when the BT network's high impedance output is set to the LSB of the GCN's input.

3. Comparison of network implementations

For a MOS implementation of the networks, binary switches can be implemented using transmission gates. For a MOS implementation of a B bit DEM DAC, the FRDEM topology requires $2^{B+3}-4B-8$ transmission gates, the equivalent GCN requires $B2^{B+1}$ transmission gates and the BT network requires $2^{B+1}+B2^B-2B-2$ transmission gates. Because $B2^{B+1} > 2^{B+3}-4B-8$ when $B > 2$ and $B2^{B+1} > 2^{B+1}+B2^B-2B-2$ when $B > 0$, both the FRDEM and the BT network implementations require fewer transmission gates than the GCN. When compared to the FRDEM network, the BT network requires fewer transmission gates when $2^{B+3}-4B-8 < 2^{B+1}+B2^B-2B-2$ or $B < 5.67$. Table 1 compares the hardware requirements of the three equivalent network topologies. The results in Table 1 show that the BT implementation requires approximately the same number of transmission gates as the FRDEM implementation for six bits. However, the physical layout of a six bit BT network has more geomet-

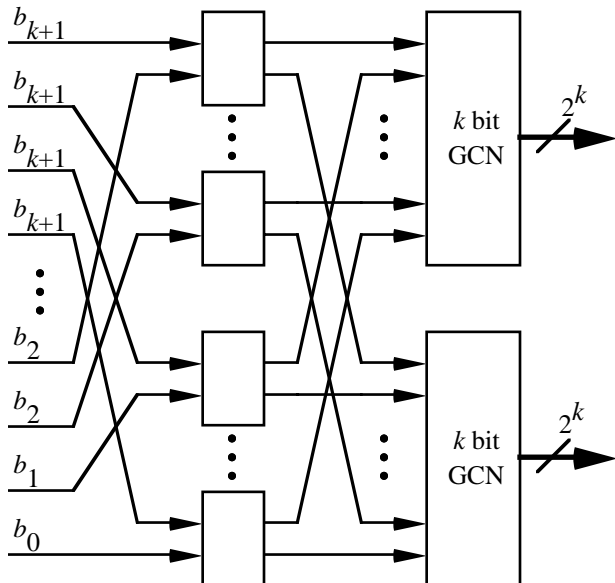


Figure 7. A partitioned $k+1$ bit GCN. The control signal, $c_k(n)$, has been omitted for clarity.

ric regularity, simpler routing and is more compact than the physical layout of a six bit FRDEM network. Thus, of the three networks, the BT network has the lowest hardware complexity for two to six bit DACs, and the FRDEM network has the lowest hardware complexity for DACs with seven bits or more.

4. Conclusions

In this paper, the FRDEM network in [3] and the BT network in [4] have been shown to be equivalent to an appropriately connected GCN. Of these three networks, the BT network requires the lowest hardware complexity for DACs with 6 bits or less, and the FRDEM network requires the lowest hardware complexity for DACs with more than 6 bits.

References

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bits	FRDEM	GCN equivalent	BT network
	transmission gates	transmission gates	transmission gates
3	44	48	32
4	104	128	86
5	228	320	212
6	480	768	498
7	988	1792	1136
8	2008	4096	2542

Table 1. Hardware complexity comparison of equivalent implementations of FRDEM