

Logic Structures Homework

- Use Technology: tsmc018.model, Vdd = 2.5 V for all problems.
- All inputs should be driven by a 1X inverter.
- All outputs should be loaded by a 4X inverter.
- For multiple input gates, always use the input that is the longest distance from the output.
- When comparing delays, use average delay $(T_{PLH} + T_{PHL})/2$

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Problem #1: Average Delay

For a chain of 10 inverters, identify via simulation the pullup/pulldown ratio that gives the smallest average delay $(T_{PLH} + T_{PHL})/2$.

Use this pullup/pulldown ratio in all subsequent static logic gates. Do not fudge even when this means very large PMOS transistors.

Use 1X sizes for everything.

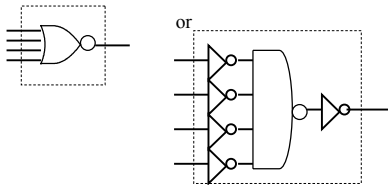
When comparing delays, compare average delay $(T_{PLH} + T_{PHL})/2$

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Problem #2: Logic Structures

Which structure is faster:



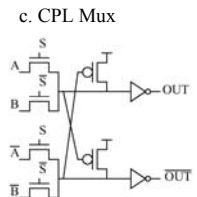
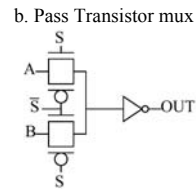
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Problem #3 Mux Structures

Which structure is faster:

a. Static CMOS Mux (you design) – output must be noninverting.



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3-Input XOR gate

Which structure is faster for XOR3:

- Full static CMOS XOR3
- XOR3 built from two XOR2 static CMOS gates
- XOR3 built from two pass-transistor XOR2 gates
- DCVSL XOR3

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