

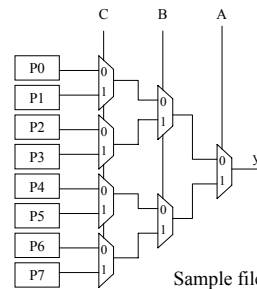
## Logic Structures Homework

- Use Technology: tsmc018.model, Vdd = 2.5 V for all problems.
- Use the testbench provided to test the design.
  - File is tb\_lut3.sp
- Top 3 designs in terms of fastest overall design gets 15 pts add to next test grade.
  - Cannot use a transistor wider than 8X minimum width.
  - When comparing delays, use average delay  $(T_{PLH}+T_{PHL})/2$
- You may not work in groups. All work is individual.

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## 3-input Lookup Table



subckt lut3

in lut3\_netlist.sp

Sample file provided uses a Verilog-A model of a mux2 for checking testbench functionality.

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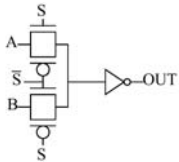
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## Mux Structures

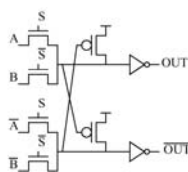
Which structure is faster when used as the mux2 circuit in the LUT3?:

a. Static CMOS Mux (you design)

b. Pass Transistor mux



c. CPL Mux



d. DCVSL MUX

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## To Do

- Implement the LUT3 circuit using the four circuit approaches on the previous page.
- Compare the speed of the designs in your report.
- Provide four files
  - lut3\_static.sp
  - lut3\_pass.sp
  - lut3\_cpl.sp
  - lut3\_dcvs1.sp
- Each file must be able to be included in the testbench file in place of lut3\_netlist.sp and provide the same functionality.

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