

## DFF Design Styles Homework

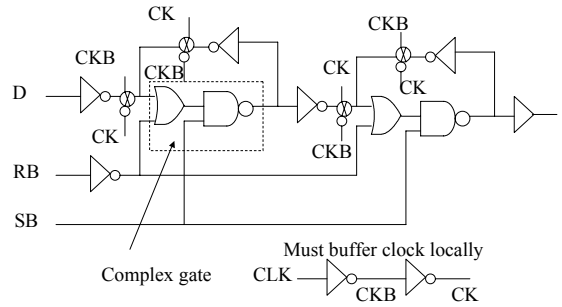
- Use Technology: tsmc018.model, Vdd = 2.5 V for all problems.
- Problem #1: Compare Tcq of two different DFF styles.
- Problem #2: Measure setup/hold of DFFs.
- Top 3 designs in terms of fastest overall design gets 15 pts add to next test grade.
  - Cannot use a transistor wider than 8X minimum width.
  - When comparing delays, use average delay  $(TCQ\_TPLH+TCQ\_TPHL)/2$

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## Static DFF

Implement the classical DFF shown below:



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## Dynamic/Static

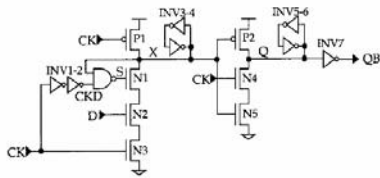


Fig. 3. Semidynamic edge-triggered flip-flop.

Implement this, add set/reset as with previous design.

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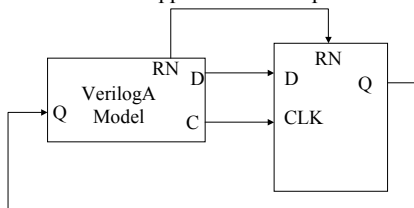
## Deliverables

- static\_tcq.sp - measure tcq for D input rising/falling, TPHL for reset input, TPLH for set input.
  - Must print out the following delays in order with these names: TCQ\_TPLH, TCQ\_TPHL, SB\_TPLH, RB\_TPHL
- dynamic\_tcq.sp - measure tcq for D input rising/falling, TPHL for reset input, TPLH for set input
  - Must print out the following delays in order with these names: TCQ\_TPLH, TCQ\_TPHL, SB\_TPLH, RB\_TPHL
- static\_tsu.sp - measure tsu for D input rising
- dynamic\_tsu.sp - measure tsu for D input rising
- static\_thd.sp - measure thd for D input rising
- dynamic\_thd.sp - measure thd for D input rising

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## One Approach for Setup/Hold Time



For every two clocks: first clock, reset DFF, 2<sup>nd</sup> clock apply D low-to-high, then CLK rising edge. Check Q after prop delay, if '1' succeeded, divide interval in half between D transition and CLK transition. After a fail, new D rising edge will be halfway between last pass and last fail condition. Exit when interval is less than 100 ps.

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