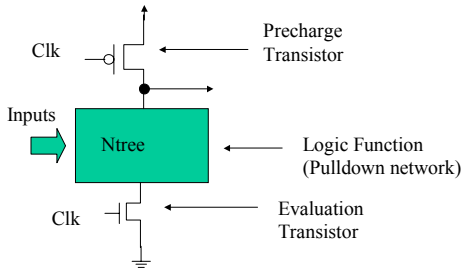


### Dynamic Gates

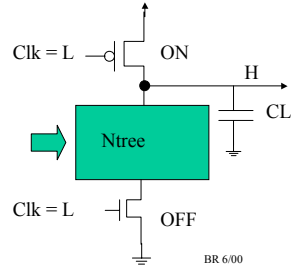


BR 6/00

1

### Operation of a Dynamic Gate

- Precharge phase: Clock Low, Precharge transistor on, output pull high. Evaluation transistor off.

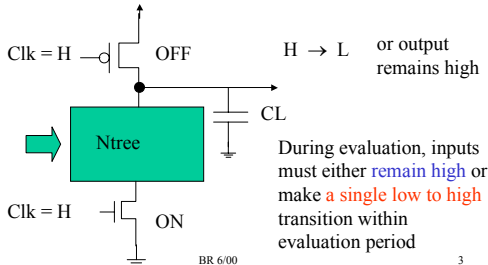


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2

### Operation of a Dynamic Gate (cont)

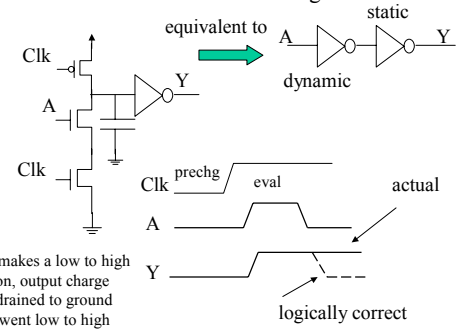
- Evaluation phase: Clock H, Precharge transistor off, Evaluation transistor on. Output is pulled low if there is a path in Ntree to ground.



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3

### Why must gate input only make a single low to high transition or remain high?

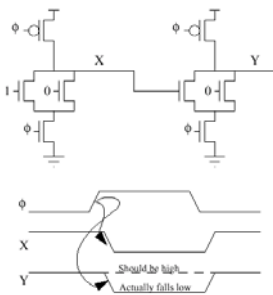


Input A makes a low to high transition, output charge already drained to ground when A went low to high

BR 6/00

4

### Cascading Dynamic Gates

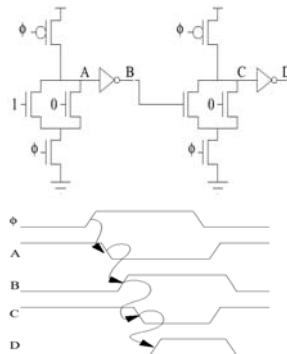


X input to 2<sup>nd</sup> gate violates transition rule and makes a high to low transition. Because X was high to begin with, charge on Y node was discharged to ground before X transitioned to 0.

BR 6/00

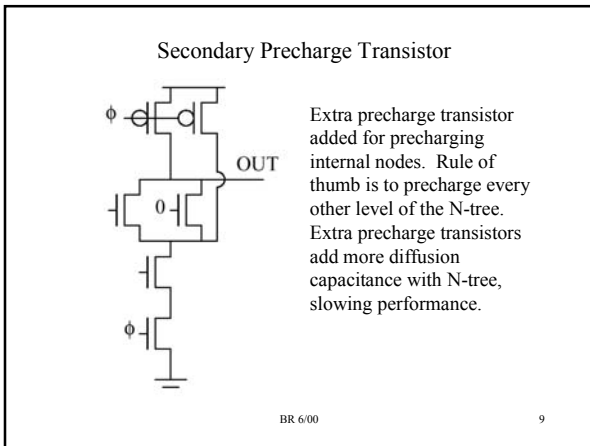
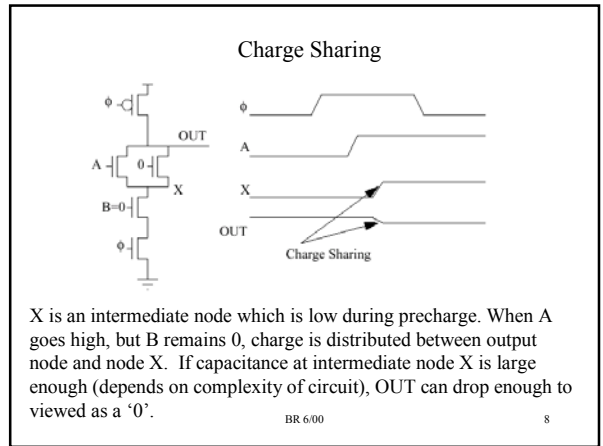
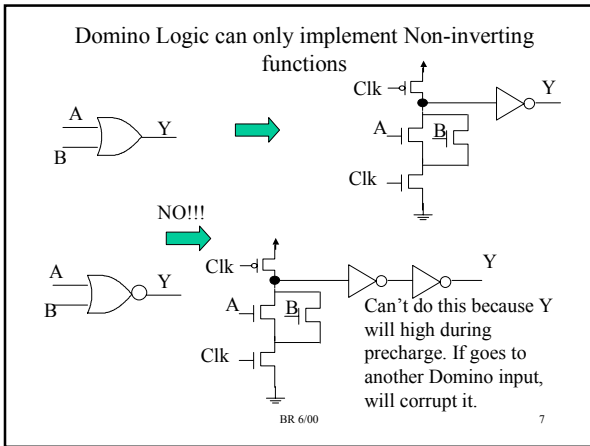
5

### Domino Logic – Place static inverter on gate output

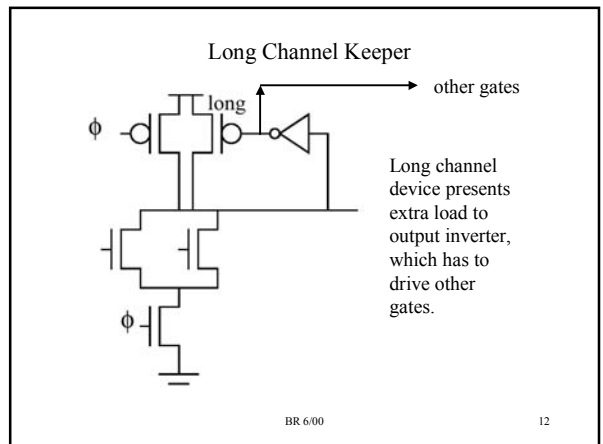
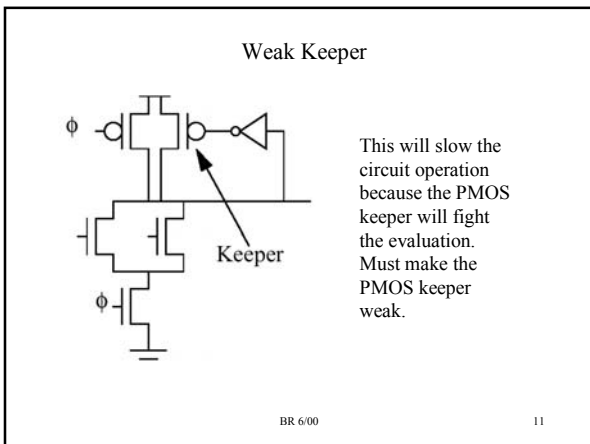


Static inverter on output ensures that inputs to cascaded gates follow monotonicity rule: inputs either remain high or make single transition low to high.

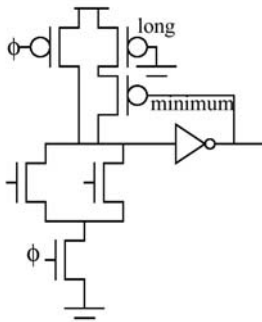
6



- ### Subthreshold Leakage
- If the clock stays high for an extended period, the output charge will leak off due to subthreshold currents
  - Dynamic circuits typically have a minimum clock frequency requirement because of this.
  - Subthreshold leakage gets worse as you scale down in technology.
- BR 6/00 10

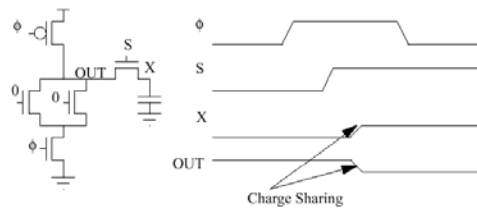


### Split Keeper



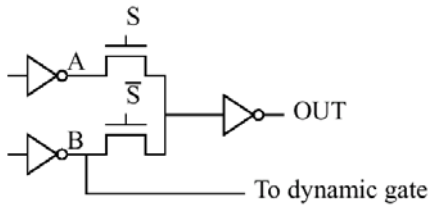
Keeper gate load now reduced on gate output.

### Charge Sharing with Pass Transistors



If S turns on during evaluation, charge at Node X can corrupt charge on dynamic gate.

### Glitching via Pass Transistors



If S and S' are on at the same time for a short period of time, nodes A, B can fight each other causing a glitch, which then could trigger a dynamic gate. Dynamic gate inputs are sensitive to glitches.

### Performance Considerations

Critical path is determined by pulldown speed of NTREE + pullup speed of inverter (Inverter Tplh). Only need to optimize the Tplh of the inverter.

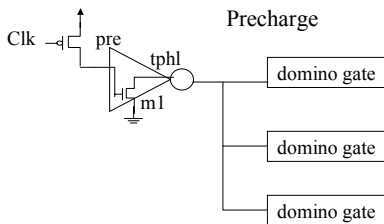
During evaluation, cascaded domino gates trigger sequentially via 0 to 1 transitions. Length of precharge period will be set by delay along longest path in the domino logic (critical path).

During precharge, all domino gates precharge in parallel.

Precharge time is not equal to Evaluate time, clock does not to be a 50% duty cycle clock (but probably is in a pipelined system)

Precharge period must be long enough so that inverter 1 to 0 transition reaches all its fanins. Size of the precharge transistor + t<sub>plh</sub> of inverter should be sized to meet precharge period.

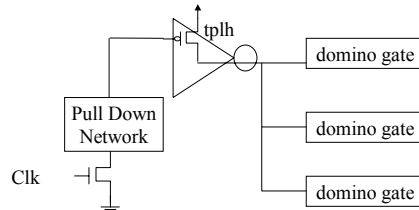
### Precharge



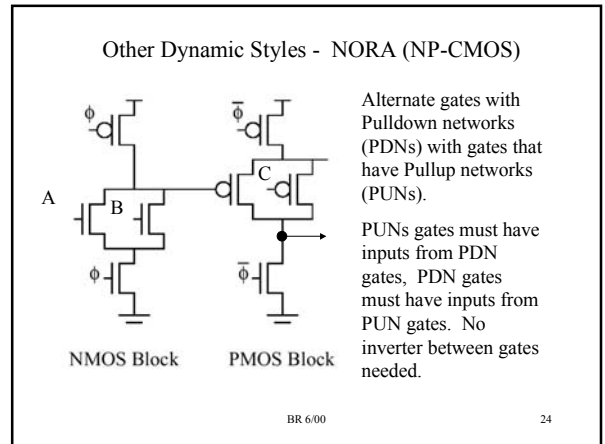
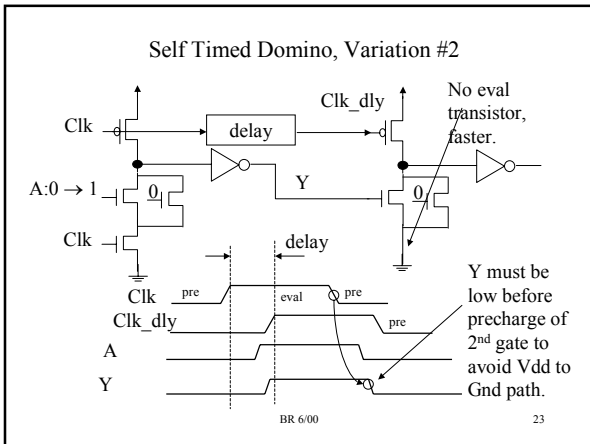
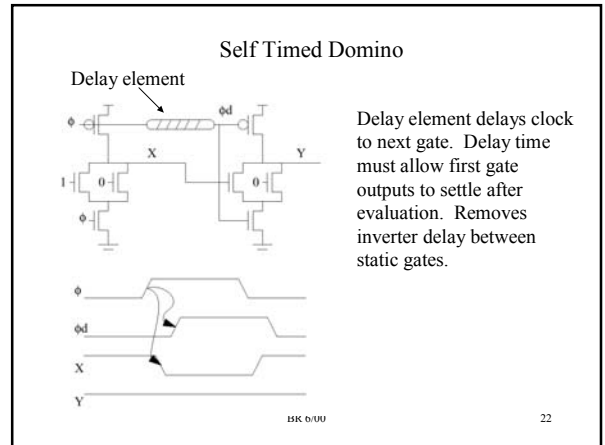
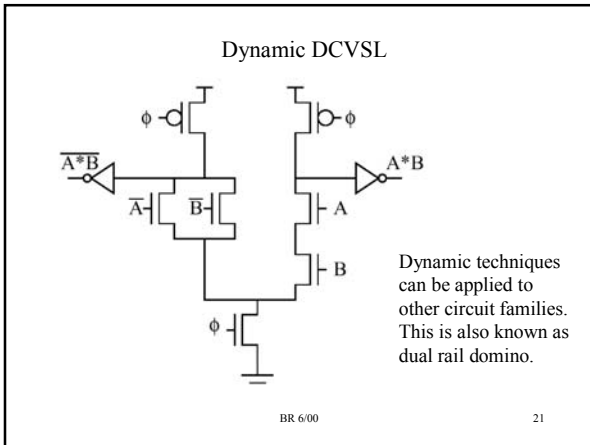
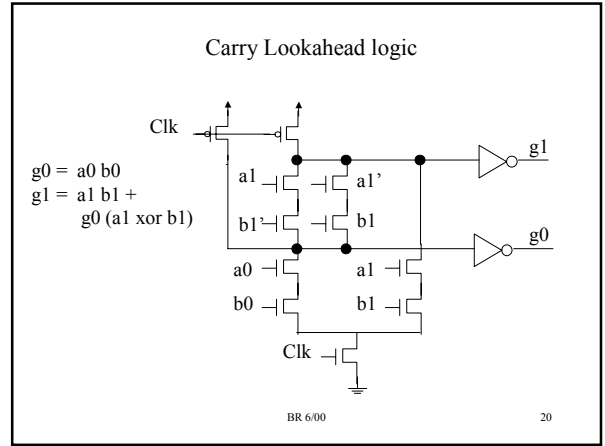
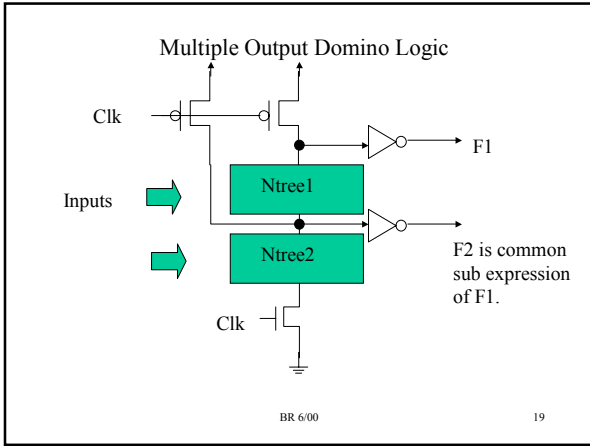
Path through  $pre+m1$  sized to meet minimum precharge period requirements.

Don't want to make  $pre$  too large because of clock loading. Don't want to make  $m1$  too large because will load 'evaluation' path.

### Eval

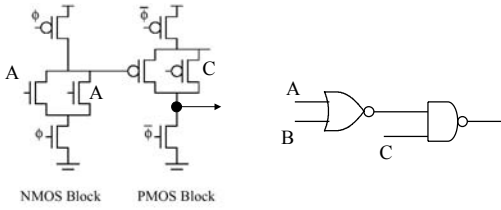


Need to optimize t<sub>plh</sub> path in inverter. Want to size the EVAL path first, then size the precharge path. If using a 50% duty cycle clock, eval time will be longer than precharge time, and will size precharge path to be equal to eval time.



### NORA (NP-CMOS)

NMOS gates evaluate when Clock is high, PMOS gates evaluate with Clock low. Can implement inverting logic.



Principle disadvantage is low noise margins. High margin is  $V_{tp}$ , Low margin is  $V_{tn}$ .