

IA-64 Generations 2,3 CPU and CLK

- This lecture uses two papers that discuss the clock and CPU design of the second and third generations of the IA-64
 - Anderson, F. E., Wells, J. S., Berta, E. Z., "The Core Clock System on the Next Generation Itanium Processor", ISSCC 2002, pp 453-456.
 - Tam, S., Desai, U., Limaye, R., "Clock Generation and Distribution for the Third Generation Itanium Processor", 2003 Symposium n VLSI Circuits, pp 9-12.
 - Stinson, J., Rusu, S., "A 1.5GHz Third Generation Itanium Processor", ISSCC 2003, paper 14.4.
 - The implementation of the Itanium 2 microprocessor**
Naffziger, S.D.; Colon-Bonet, G.; Fischer, T.; Riedlinger, R.; Sullivan, T.J.; Grutkowski, T.;
 Solid-State Circuits, IEEE Journal of , Volume: 37 Issue: 11 , Nov. 2002
 Page(s): 1448 -1460
- All notes in this lecture are from these four papers.

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Clock Comparison of three generations

Table 1:

| Attribute | First Generation | Second Generation | This Work |
|-----------------------------|---|---|---|
| Process/Metal | 180nm / Al | 180nm / Al | 130nm / Cu |
| Clock Distribution Topology | H-Tree global clock & independent zonal clock grids | H-tree global clock and tree based zonal clocks | H-tree global clock and tree based zonal clocks |
| De-skew method | Active (non-continuous) | None | Fuse based |
| Clock Skew | 28 ps | 62 ps | 24 ps (fuse based de-skew) 7 ps (SCAN based de-skew) |

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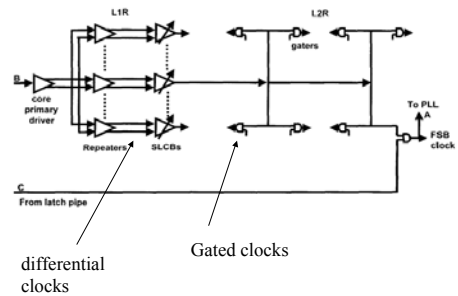
Comments

- Active de-skewing used in 1st generation jettisoned in 2nd generation
 - 2nd generation just used a balanced H-tree
 - Difficult to route this type of structure - all clock routing was reserved prior to block layout
 - Differential clocks used for 2nd level clock distribution - reduced jitter
 - Non-active de-skew easier to test, and more deterministic behavior
 - Intentional clock skewing for time borrowing easier
- 3rd generation uses programmable fuses for skewing
 - allows skew adjustment after fabrication

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2nd Generation Clock distribution



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2nd Generation Second Level Clock Buffer

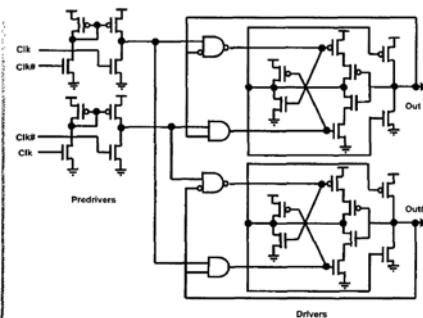
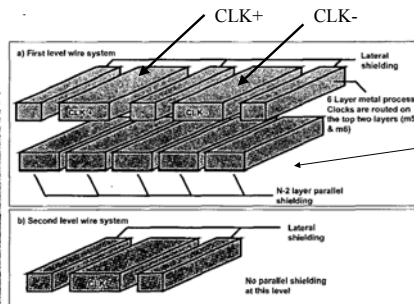


Figure 8.5.3: Primary driver/repeater/SLCB schematic.

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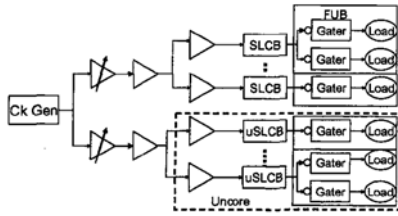
2nd Generation Clock Shielding



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3rd Generation Distribution



PLL → MPD → PD → RPTR → SLCB → Gater

Figure 2: Clock Distribution Hierarchy

Copper interconnect used, extra performance headroom

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Fuse-Based De-skewing

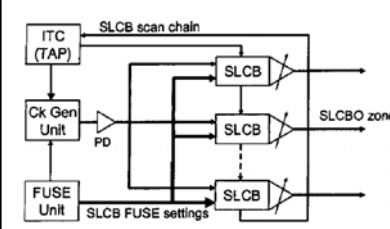


Figure 5: Fuse Based SLCB Architecture

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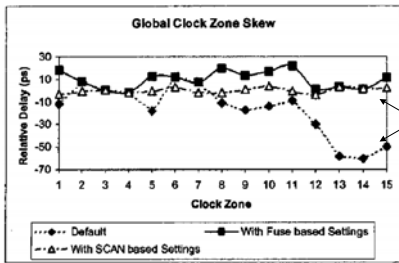
69 fuses controlling 23 clock zones.

Delay increments in 30.5 ps over 220 ps range.

Exhaustive search for best fuse settings not possible, use a generic search algorithm with statistical history to help; done during production sort.

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Results of Skew Adjustment



Made a big difference here. Skew reduced from 60ps to 24 ps.

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IA-64 CPU Comparison

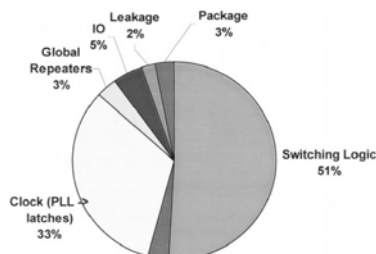
| Attribute | Itanium® [2] | Itanium®2 [3] | This work |
|-----------------|---|---------------|-----------|
| Architecture | Explicitly Parallel Instruction Computing | | |
| Process | 180nm | 180nm | 130nm |
| Device Count | 25M | 221M | 410M |
| On-die L3 cache | 0* | 3MB | 6MB |
| Frequency | 800MHz | 1.0GHz | 1.5GHz |
| Supply Voltage | 1.6V | 1.5V | 1.3V |
| Power | 130W* | 130W | 130W |

* Includes 4MB cache on cartridge

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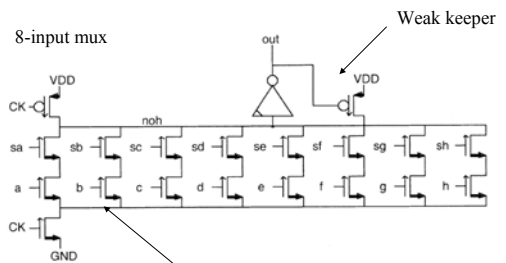
Power Distribution in 2nd Gen IA-64



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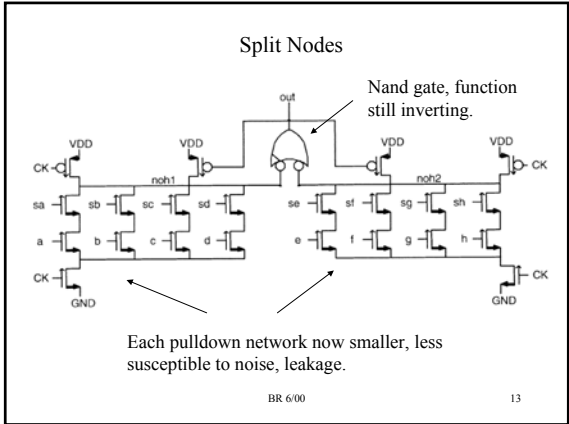
Domino Mux in 2nd Gen



Multiple parallel paths, more susceptible to noise, leakage.

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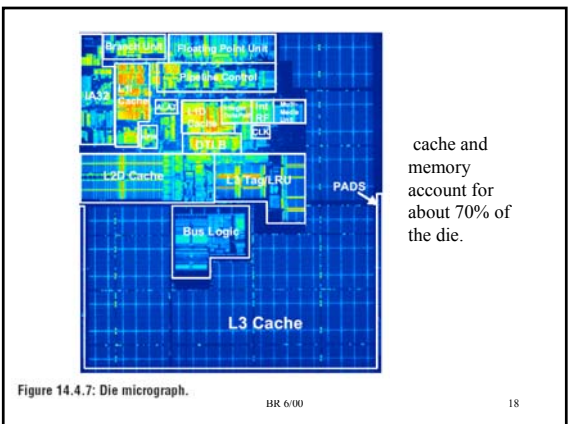
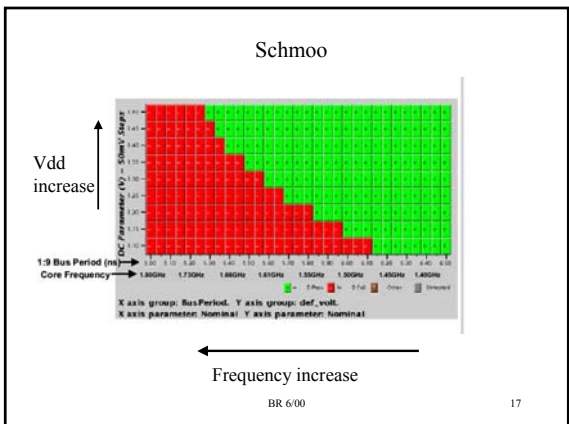
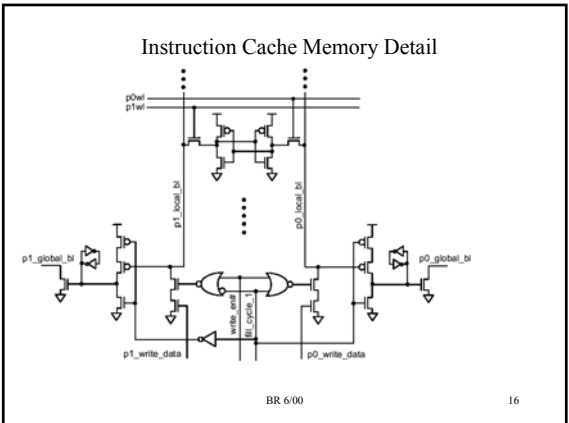
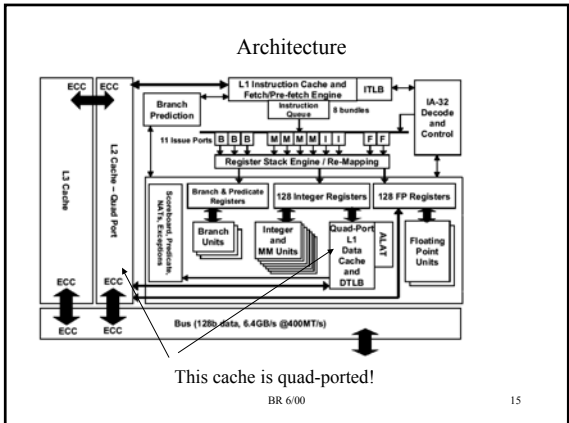
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| Attribute | Value |
|-------------|---------------------------|
| Gate Leff | 70nm |
| M1 pitch | 350nm |
| M2 pitch | 448nm |
| M3 pitch | 448nm |
| M4 pitch | 756nm |
| M5 pitch | 1120nm |
| M6 pitch | 1204nm |
| Dielectric | FSG, K=3.6 |
| Memory cell | 2.45 μ m ² |

Process For 3rd Generation

Figure 14.4.1: 0.13 μ m process characteristics. BR 6/00 14



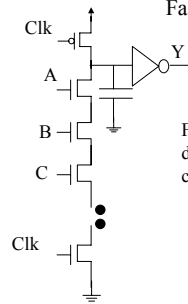
Other Features

- Register File 128x65, 20 ports!
- Latency of 3rd level cache is 14 clocks, latency of 2nd level is 6 clocks

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Fast 'AND' Logic



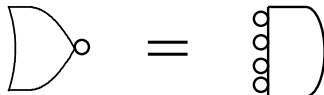
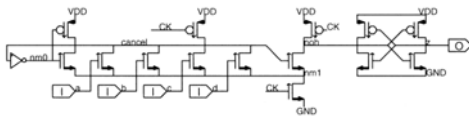
Fast AND gates required for decoders, also handy for some computation types ($X=0?$)

Each new AND input requires another N-transistor in series, high-fanin AND gates are slow.

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Annihilation Gate (Flying NOR)



OR with low true output (NOR)

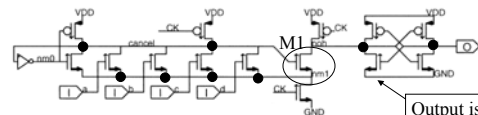
AND with low true inputs

Recall that domino logic can only implement non-inverting functions, yet here is a dynamic gate implements a NOR function.

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Annihilation Gate - Functionality



Inputs must be stable for a setup and hold time around rising clock edge; as such this acts like a rising edge-triggered device. Inputs should come from static logic, acts as static-to-dynamic converter.

Connection points added for emphasis.

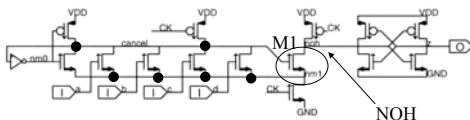
During precharge, high nodes: cancel, nm1, noh

Output is low. M1 is on.

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Annihilation Gate - Functionality (cont)



For eval, CK 0 \rightarrow 1 transition

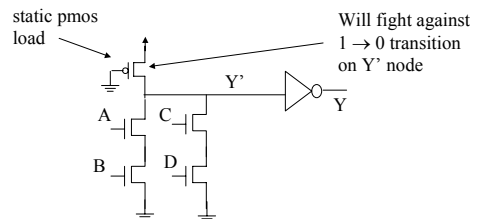
If ALL inputs are '0', then NOH 1 \rightarrow 0, and output 0 \rightarrow 1. Note this is a FAST clock-to-Q path.

If any input is '1', then the output 0 \rightarrow 1 is annihilated or canceled by the cancel signal 1 \rightarrow 0, turning off M1. The cancel signal 1 \rightarrow 0 and M1 turnoff MUST happen before the NOH node has drooped significantly to cause a 0 \rightarrow 1 output transition. This is essentially a race condition, and careful design is needed (Intel calls this a *tricky* circuit, which is an understatement).

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Pseudo-NMOS



Less capacitive loading on inputs, faster than static CMOS, but will consume static power when N-tree is pulling down.

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