

### Can we get rid of transmission gates?

Pullups fully up to VDD (*level restorer*).

Complementary Pass Transistor Logic (CPL). Dual rail logic, twice as many signals as normal.

Sizing of PMOS will not cause incorrect circuit operation, only effect speed of falling transitions.

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### Getting rid of Complementary Gate

Must be careful to size PMOS weak enough to be overdriven by input. Performance degrades in submicron technologies.

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### Summary of Pass Transistor Logic

- Works well for mux logic
- Best choice is CPL with level restoring PMOS pullups
  - Can get rid of level restoring PMOS pullups with special 'low threshold' pass transistors. Requires support at process level.
- Layout can be difficult for pass transistors
- CPL dual rail requirements doubles routing requirements, and the area of most current designs are already more wiring limited than transistor limited.

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### Sizing of Pass Transistors

Increasing W/L will decrease R, but will increase Source/Drain Cap

$$\text{Delay} = R_{\text{pass}} * (C_{\text{pass}} + C_{\text{load}})$$

$$= R_{\text{pass}} * C_{\text{pass}} + R_{\text{pass}} * C_{\text{load}}$$

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### Sizing of Pass Transistors

W/L ??

$$\text{Delay} = R_{\text{pass}} * (C_{\text{pass}} + C_{\text{load}})$$

$$= R_{\text{pass}} * C_{\text{pass}} + R_{\text{pass}} * C_{\text{load}}$$

Constant with increasing W.      Decreasing with increasing W.

If  $C_{\text{pass}} \ll C_{\text{load}}$ , then get overall speed increase from increasing W. If  $C_{\text{pass}} > C_{\text{load}}$ , then little benefit from increasing W

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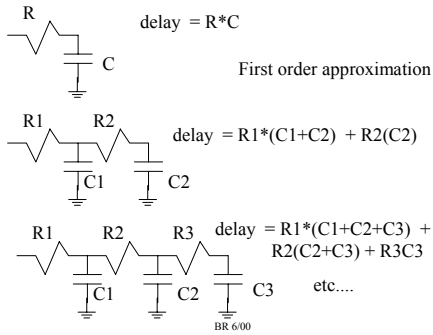
### Example

Larger than minimum size will result in higher speed.

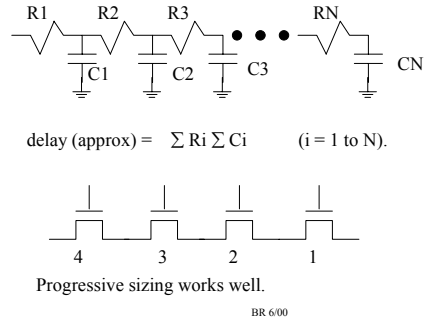
How do we size these transistors???

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### Elmore Delay



### Elmore Delay (cont)



### Manchester Carry Chain (Pass transistor chain)

See Figure 11.9 in Rabaey Textbook, pg 569

Sum = A xor B xor Ci

Cout = (A and B) or (B and Cin) or (A and Ci)

Define Generate, Propagate signals:

Generate true if FA block generates a carry.

$G_i = A \text{ and } B$

Propagate true if FA block propagates a carry

$P = A \text{ or } B$

Sum = P xor Ci

Cout = G + (P and Cin) Carry chain is critical path.

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