Skewed CMOS

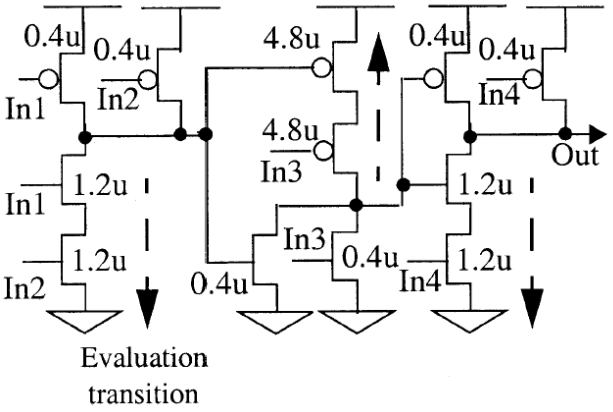
- Notes are taken from:
  - **Skewed CMOS: noise-tolerant high-performance low-power static circuit family**
    Solomatnikov, A.; Somasekhar, D.; Sirisantana, N.; Roy, K.;
    Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 10 Issue: 4 , Aug. 2002
    Page(s): 469 -476

Skew CMOS: Goals

- Large performance gap between dynamic logic and static logic
  - Dynamic logic high performance but high power as well due to clock load. Also more susceptible to noise issues
  - Static CMOS easy, but low performance. Has good noise tolerance.
- Want a logic family that has best characteristics of both dynamic and static logic
  - Skewed CMOS claims to have nearly the performance of domino logic, but with half to 1/3 the power of domino logic.
  - Also claims better noise tolerance

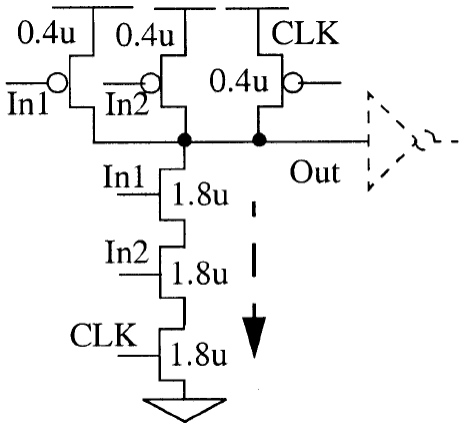
Approach

Basic idea is simple: Design a static skewed logic family that favors one transition over the other. Intersperse logic levels at regular intervals (2-3 gate intervals) with gates that have precharge capability so that can take advantage of fast transitions.



arrows indicate fast transitions during evaluation

Precharge Gates



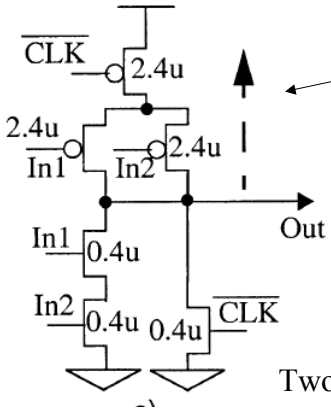
Precharge gates used to speed up resetting to state for fast evaluation.

Precharge used to overcome 'slow' path in gates.

Note this family can implement inverting logic!

NAND gate with fast precharge to VDD

Precharge Gates (cont)



Fast evaluation path is to VDD.

Two input NAND with fast precharge to GND.

Performance

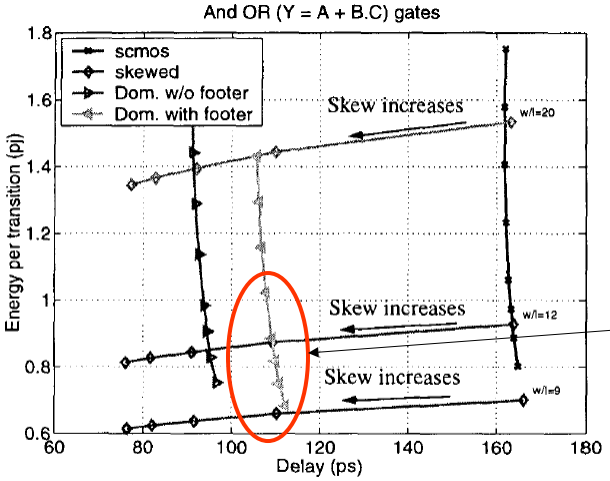


Fig. 8. AND-OR energy vs. delay

w/o footer means no evaluation transistor.

Performance competitive/better than Domino.

Pipeline Structure

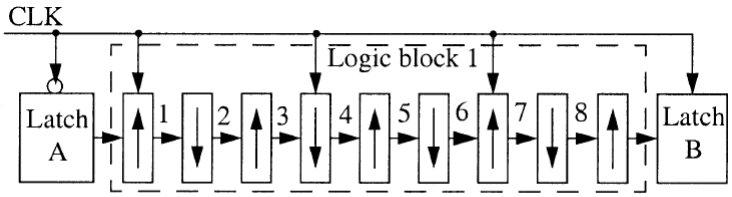


Fig. 5. Logic block structure.

Note that precharge blocks are only about one out of every three blocks – this means 1/3 the clock load, less power.

Pipeline Structure (cont).

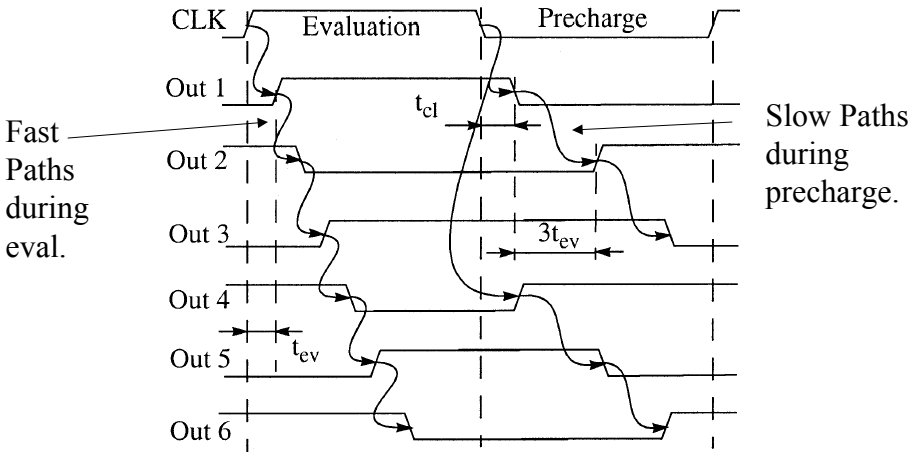
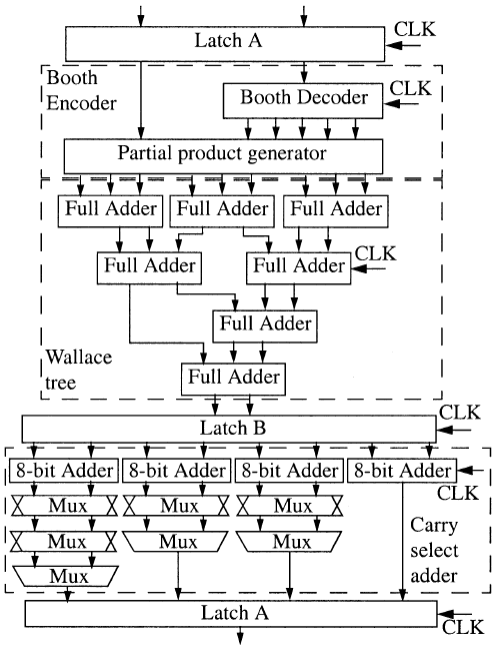


Fig. 6. Waveforms for circuit in Fig. 4.



Multiplier

16x16 Booth Multiplier

Note positioning of clock within skewed logic stages.

9