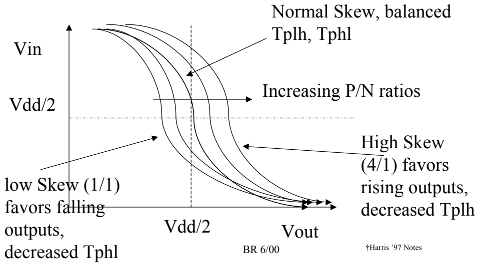
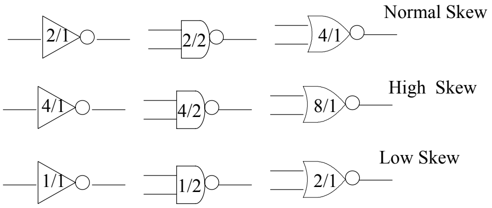
Improving Average Delay†

A question: Should the DC switching point of a static CMOS gate always be set at Vdd/2? Recall the DC switching characteristic of a static Inverter



†Harris '97 Notes

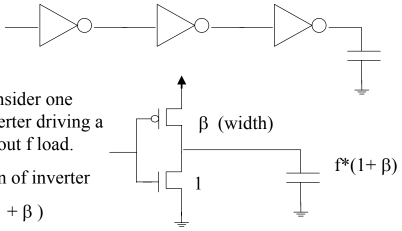
Gate Sizes and Skew



Use skewed gates when trying to speed up a particular output transistion along a critical path.

Minimum Average Delay

What should the skew be to minimize average delay in a string of inverters driving a load?



Consider one inverter driving a fanout f load.

(Cin of inverter

= 1 + β)

Minimum Average Delay (cont)

Average delay = (Tplh + Tphl)/2

Recall RC model time model:

Tp = Tnoload + K*Cload

where is K is inversely proportional to channel width (represents channel resistance).

We can ignore Tnoload for this analysis.

Tphl (falling delay) proportional to 1*f (1 + β)

Tplh (rising delay) proportional to k/ β *f (1 + β)
where 'k = B' for the case of Tplh = Tphl. 'k' accounts for differences in P/N mobility.

Minimum Average Delay (cont)

Average delay = (Tplh + Tphl)/2

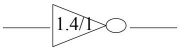
$$= (k/\beta * f(1+\beta) + f(1+\beta))/2$$

$$= f(1+\beta)(k/\beta + 1)/2$$

To find best value for β , take derivative and set to 0:

$$d\,\mathit{delay}/d\beta = f/2\,(1 - k/\beta^{2}) = 0$$

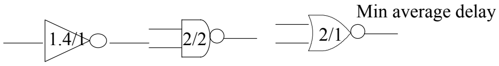
$$\beta = \text{sq\_root}(k)\ !!!$$



Minimum average delay

Trades off some Tplh time for overall decreased loading.
Saves power as well!

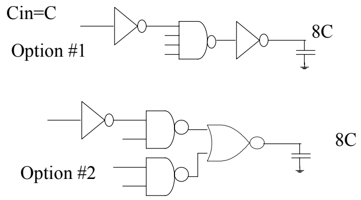
Minimum Average Delay



These gates sized for minimum average delay.

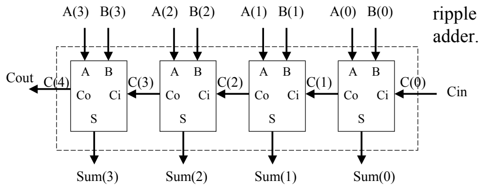
Topology Selection

Which is better? We have seen that logical effort may be able to help us make this choice, but usually simulation is needed. Right choice is technology dependent!!!!



Critical Inputs

In general, late arriving inputs should drive inputs that are close to the output, early arriving inputs should drive inputs that are close to the rail. For example – in a full adder cell, carry input should be close to output (Fig 11-6 pg 567, Rabaey).

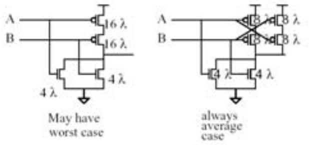


4-bit ripple adder.

If Arrival times are unknown....

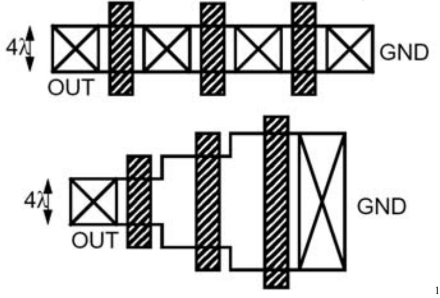
If arrival times are unknown, and you need to fold the transistors anyway, can use the following trick:

FIGURE 11. Twisting stacks for average delay



Stack Tapering

Increasing width of transistors near rail can improve delay. Benefits at sub-micron geometries are somewhat marginal.



Summary of Static CMOS Features

- Very robust – i.e, “almost idiotproof” (Harris quote!)
- Very low DC leakage (nearly zero)
- Low AC power
- Scales well to low voltage
- Handled well by synthesis tools and simulators
- Well understood

Should be the default case for logic implementation unless special needs dictate some other family.