

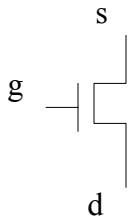
# Principles of VLSI Review

- Static CMOS Logic Design
- Delay Models
- Power Consumption
- CMOS Technology Scaling

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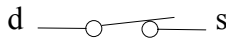
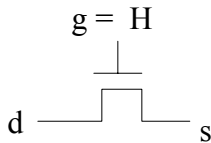
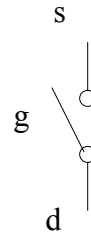
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## CMOS Transistors (N-type)

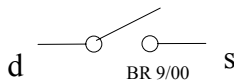
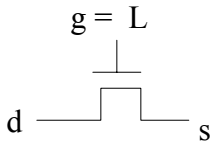


N-type (NMOS) transistor -  
can think of it as a switch.

g: gate, d: drain, s: source



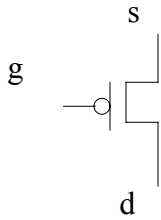
When  $g = H$ ,  $d$  is connected to  $s$  (current flows between  $s, d$  because switch is closed).



When  $g = L$ ,  $d$  is disconnected from  $s$  (current does not flow between  $s, d$  because switch is open.)

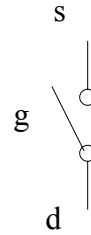
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# CMOS Transistors (P-type)

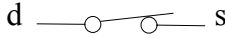
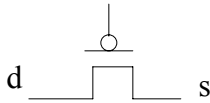


P-type (PMOS) transistor -  
can think of it as a switch.

g: gate, d: drain, s: source

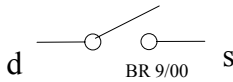
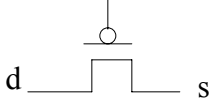


$g = L$



When  $g = L$ , d is connected to s (current flows between s, d because switch is closed).

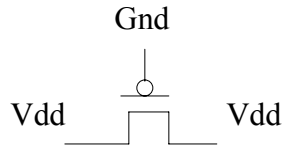
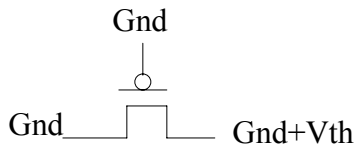
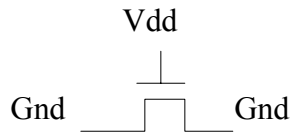
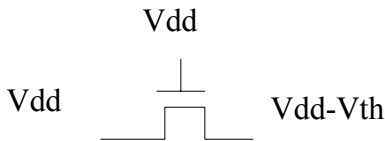
$g = H$



When  $g = H$ , d is disconnected from s (current does not flow between s, d because switch is open).

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## Reality

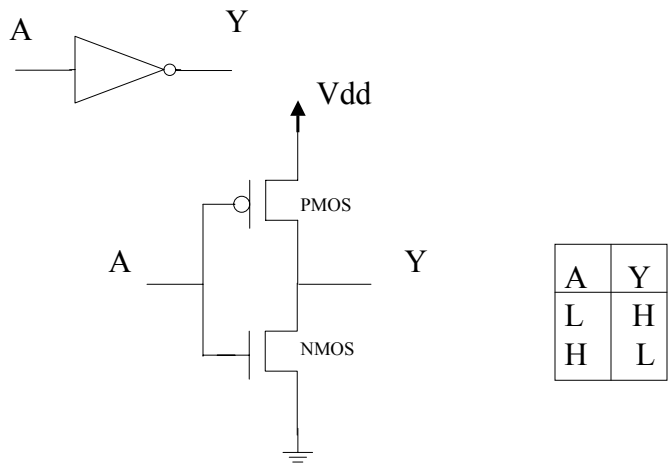


$V_{th}$  = threshold voltage

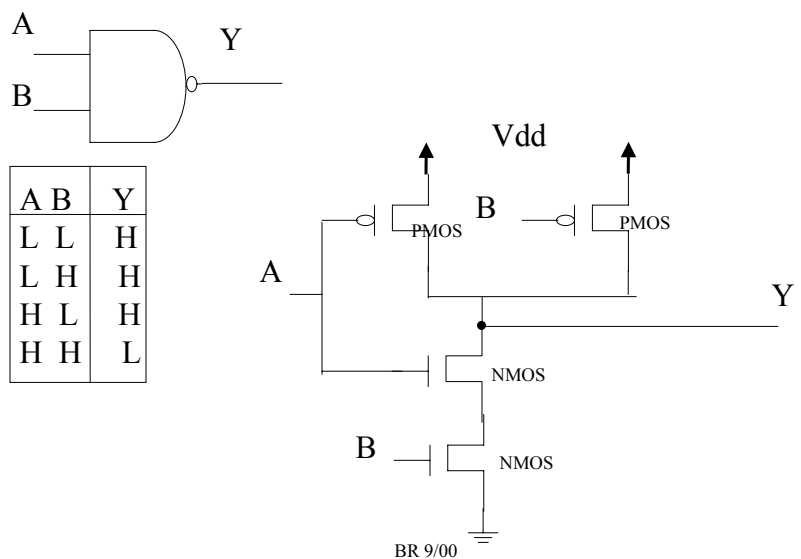
Want NMOS pulling to GND, PMOS pulling to Vdd

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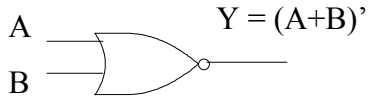
## Inverter gate - takes 2 Transistors



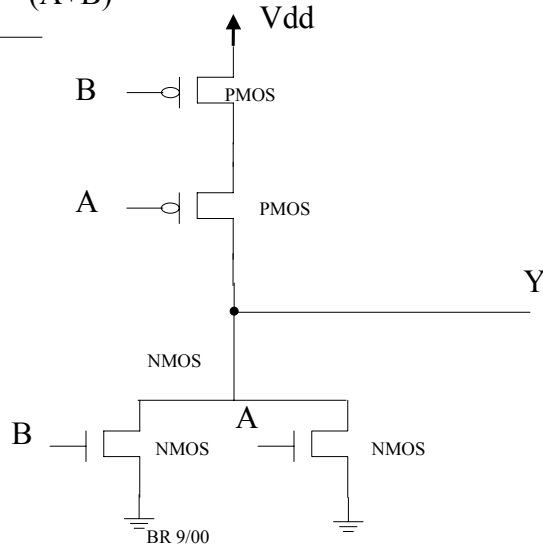
## NAND gate - takes 4 Transistors



## NOR gate - takes 4 Transistors

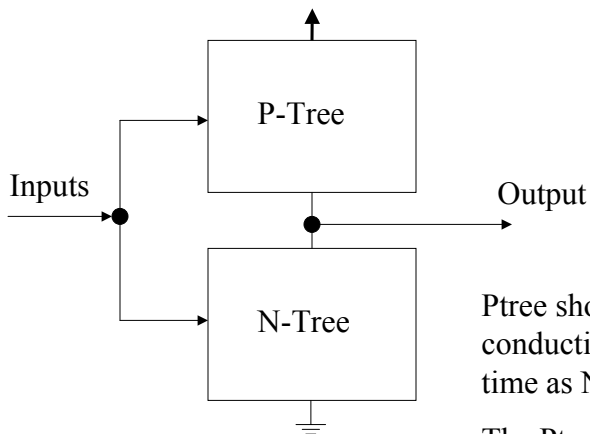


A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L



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## General Static CMOS Gate



Ptree should never be conducting at the same time as Ntree.

The Ptree and Ntree are logic *duals* of each other.

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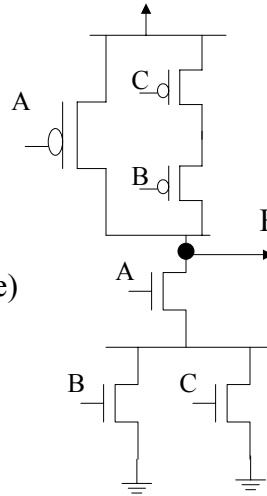
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# Complex Gate

$$F = \text{Not} (A \text{ and } (B \text{ or } C)) \quad (\text{Ntree})$$

$$F \text{ Dual} = \text{Not} (A' \text{ or } (B' \text{ and } C')) \quad (\text{Ptree})$$

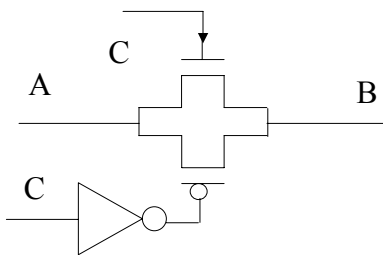
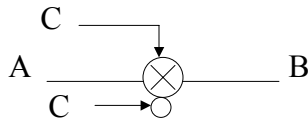
Dual: Replace Ands with Ors, Ors with Ands, complement inputs.



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# Transmission Gate

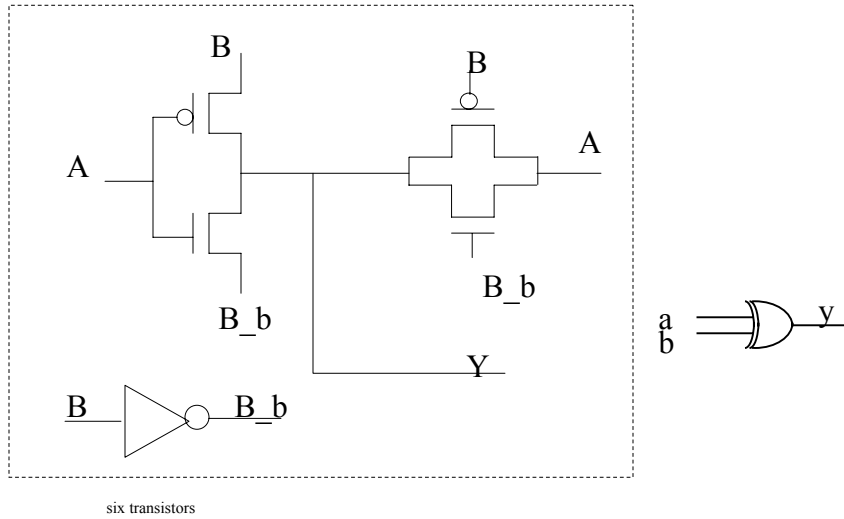


Full Vdd to Gnd  
swing between A, B

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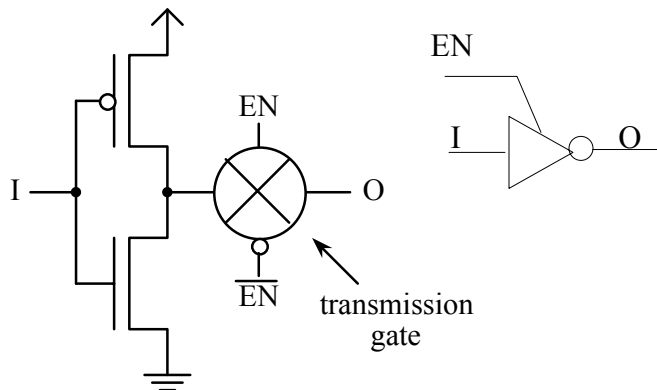
## xor2 implementation



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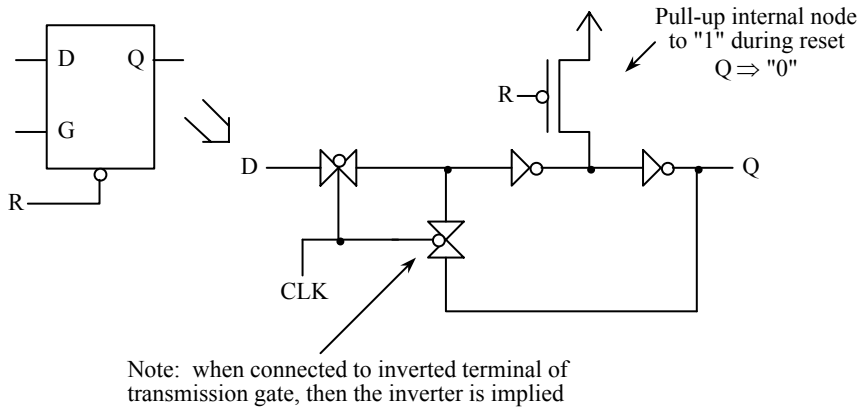
## Tristate Inverter



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## D-Latch



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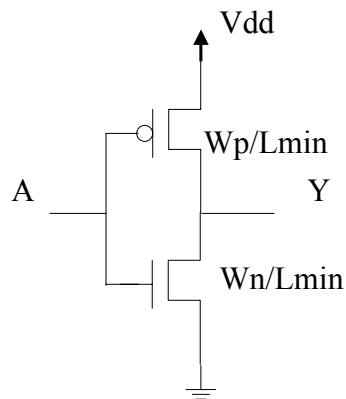
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## Lmin, Lambda

Typically for digital circuits, gate length of transistors are all the same and will be the minimum gate length allowed for that technology. Typically the number used to describe the technology is the minimum gate length.

1.2U  $L_{min} = 1.2U$   
 0.8  $L_{min} = 0.8U$   
 0.25  $L_{min} = 0.25U$

A scaling factor called *lambda* is often used to specify W/L values in a technology independent manner. Typically,  $\text{Lambda} = \frac{1}{2} L_{min}$  (not always, we will discuss this in our class).



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## Inverter Switching Point

- The inverter switching point is determined by the ratio of the  $B_n/B_p$ , where  $B_n$  is the gain of the N-tree and  $B_p$  is the gain of the P-tree.
  - If  $B_n/B_p = 1$ , then switching point is  $V_{dd}/2$
- If the  $W/L$  of both N and P transistors are equal, then  $B_n/B_p = \mu_n/\mu_p = \text{electron mobility/hole mobility}$ 
  - This ratio usually between 2 and 3
  - This means that ratio of the  $W_{ptree}/W_{ntree}$  needs to be between 2 and 3 in order for  $B_n/B_p$  to be approximately 1
- In this class will use  $W_{ptree}/W_{ntree}$  to be 2

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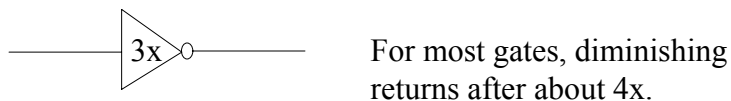
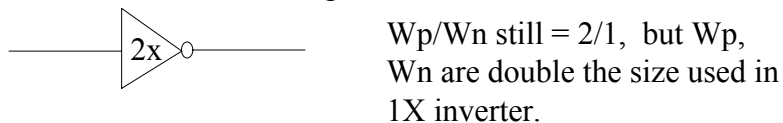
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## Gate Sizes

Assume minimum sized inverter is  $W_p/W_n = 2/1$ ,  $L = L_{min}$ .  $W_n = L_{min}$ ,  $W_p = 2 * L_{min}$ . This becomes the 1X inverter for this technology.



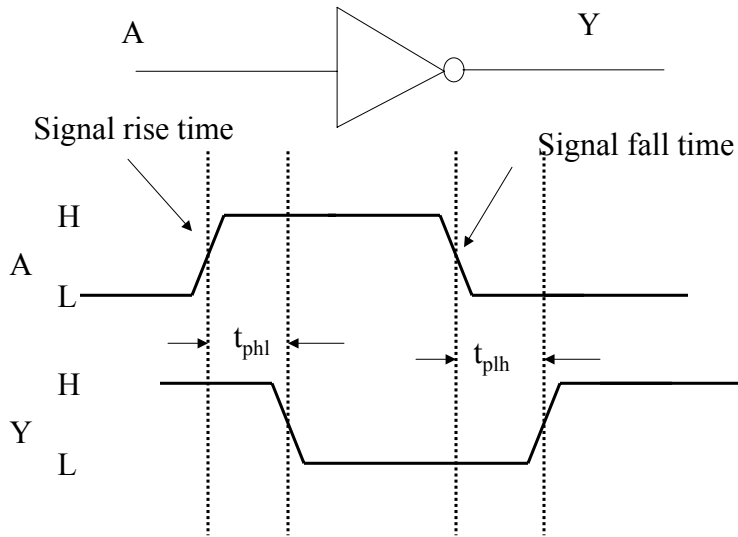
In a standard cell library, will have different sized gates to choose from for increasing loads



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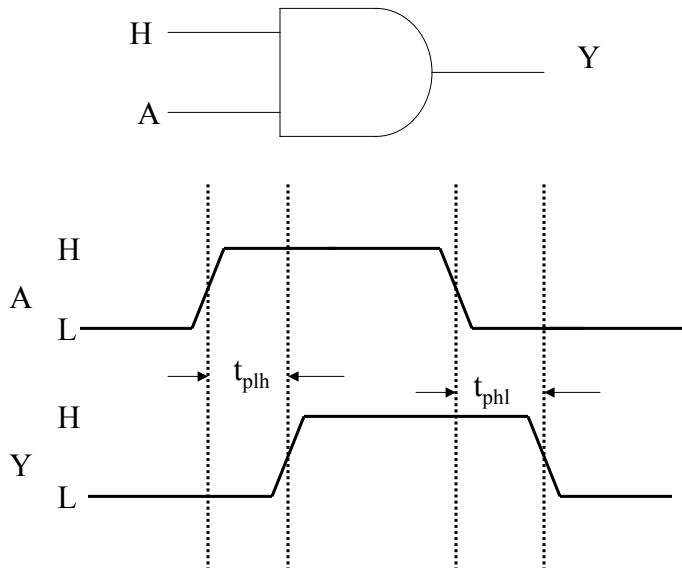
## Propagation Delay (inverting)



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## Propagation Delay (non inverting)



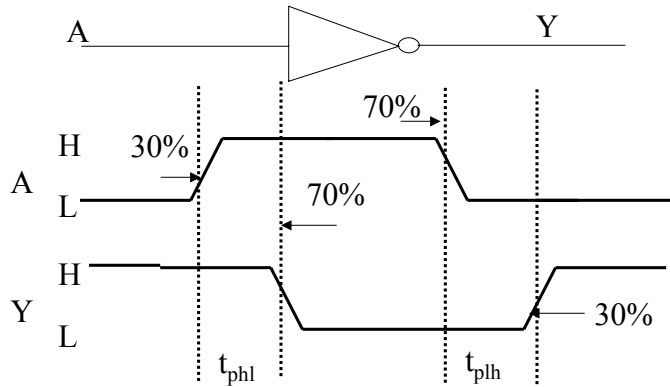
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## Where to measure delay?

If use 50% point (input) to 50% point (output), can produce negative delays (slow input slope, fast output slope).

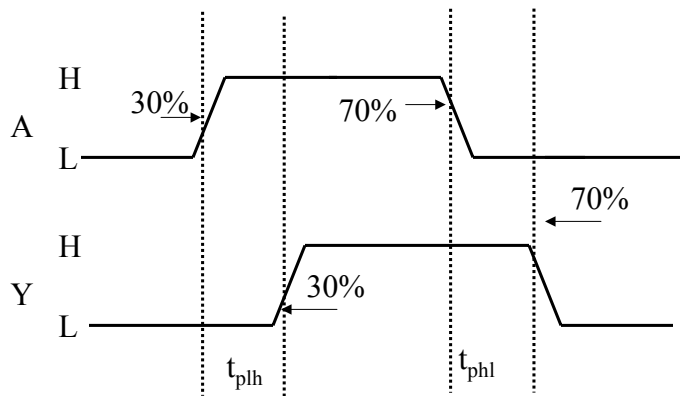
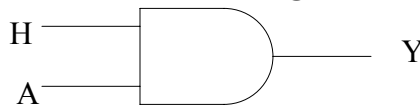
A better way is to use the 30% and 70% points on the signals.



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## Non-Inverting Gate



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## What affects gate delay?

- Environment
  - Vdd – increasing VDD decreases delay
  - Temperature – decreasing Temp decreases delay
  - Fabrication effects – Fast NMOS, Fast PMOS, Slow NMOS, Slow PMOS
- Usually measure delay for at least three cases
  - Best - high Vdd, low Temp, Fast N, Fast P  
(use high Vdd, Low temp only if these conditions can adversely affect the circuit operation, e.g. timing margin for hold time is affected by fastest paths, not slowest paths).
  - Worst - low Vdd, high Temp, Slow N, Slow P - used for determining timing margin purposes.
  - Nominal - nominal Vdd, Room Temp (25 C), nominal N,P

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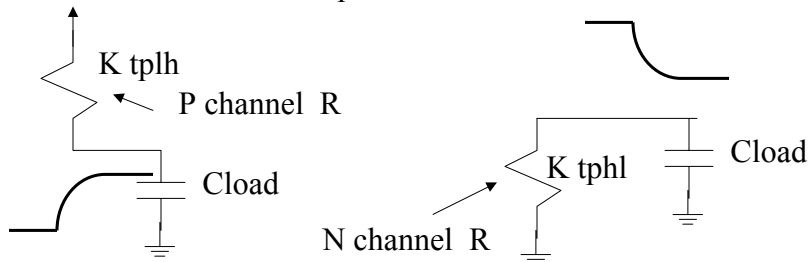
## What else affects gate delay?

Input slew and output load both affect timing. For a FIXED input slope, FIXED environment, a simple timing model is:

$$\text{delay} = T_{\text{load}} + K * \text{Cload}$$

$T_{\text{load}}$  is the delay of the gate with no external load.

K is different for TPLH, TPHL since it represents the channel resistance. Same equation is used for Slew values.



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## Table Lookup for Different Input Slews

Tplh Table (delay)

Slope	K
S <sub>1</sub>	K <sub>1</sub>
S <sub>2</sub>	K <sub>2</sub>
S <sub>2</sub>	K <sub>3</sub>
S <sub>3</sub>	K <sub>4</sub>
S <sub>4</sub>	K <sub>5</sub>

Tplh Table (slew)

Slope	K
S <sub>1</sub>	K <sub>1</sub>
S <sub>2</sub>	K <sub>2</sub>
S <sub>2</sub>	K <sub>3</sub>
S <sub>3</sub>	K <sub>4</sub>
S <sub>4</sub>	K <sub>5</sub>

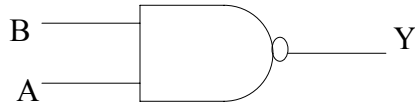
Also need tables for delay, slew for Tphl.

## 2D Table Based on Clload

Slope	Clload		
	1X CL	5X CL	15X CL
S <sub>1</sub>	K <sub>1_1x</sub>	K <sub>1_5x</sub>	K <sub>1_15x</sub>
S <sub>2</sub>	K <sub>2_1x</sub>	K <sub>2_5x</sub>	K <sub>2_15x</sub>
S <sub>3</sub>	K <sub>3_1x</sub>	K <sub>3_5x</sub>	K <sub>3_15x</sub>
S <sub>4</sub>	K <sub>4_1x</sub>	K <sub>4_5x</sub>	K <sub>4_15x</sub>
S <sub>5</sub>	K <sub>5_1x</sub>	K <sub>5_5x</sub>	K <sub>5_15x</sub>

Would need four tables for Tplh (delay), Tplh (slew), Tphl (delay), Tphl(slew)

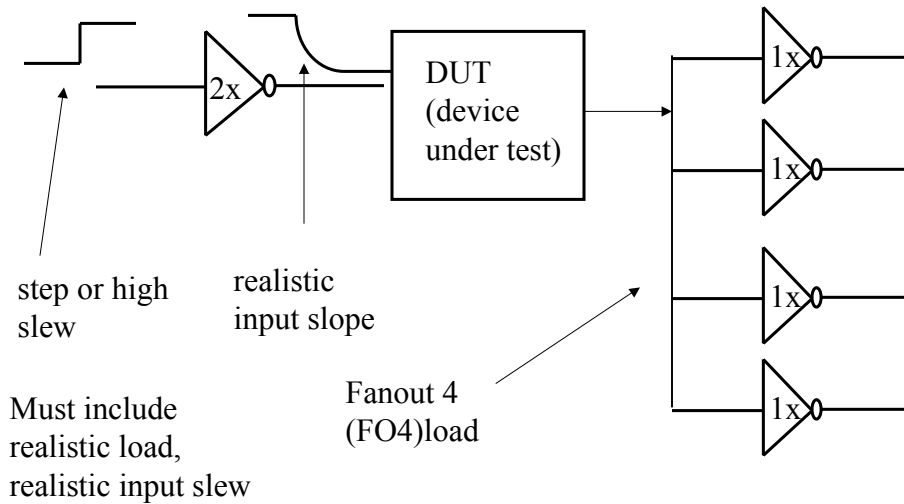
## Multiple Input Gates



Timings are  $A \rightarrow Y$   $T_{plh}$ ,  $A \rightarrow Y$   $T_{phl}$ ,  $B \rightarrow Y$   $T_{plh}$ ,  $B \rightarrow Y$   $T_{phl}$

Would need delay tables for each of these timings.

## Timing Characterization Setup



## Power Consumption In CMOS

- Static Consumption
  - Ideally, static CMOS gates with P-Tree/N-trees that are duals of each other should have negligible power consumption
  - Unfortunately, as devices have shrunk, sub-threshold current has increased and static power consumption has increased to significant values, even for static CMOS
- Dynamic Power Consumption
  - Power consumed during switching (due to signal transitions)

## Dynamic Power Consumption

$$P_d = V_{dd}^2 * \text{Cap (switched)} * \text{Frequency}$$

Switched capacitance is the capacitance that charges/discharges during a clock cycle or a computation. Includes MOSFET capacitances, routing capacitance.

Note that the biggest influence is  $V_{dd}$ . Power consumption will be reduced by the square of  $V_{dd}$  if Frequency is constant.

## Direct Path Current

There is also a '*Direct Path*' power component (short circuit current) that is due to both  $N_{tree}$ ,  $P_{tree}$  being momentarily on during switching.

Influenced by Rise/Fall time of input signals.

$P_{direct\ path} = V_{dd} * I_{peak} (T_{rise} + T_{fall}/2)/Frequency$

$I_{peak}$  is the saturation current of the  $P_{tree}$  and  $N_{tree}$  and is proportional to the size of the transistors.

We will ignore this contribution in this class.

## System Power Consumption

$System\ P_d = Static + Dynamic$

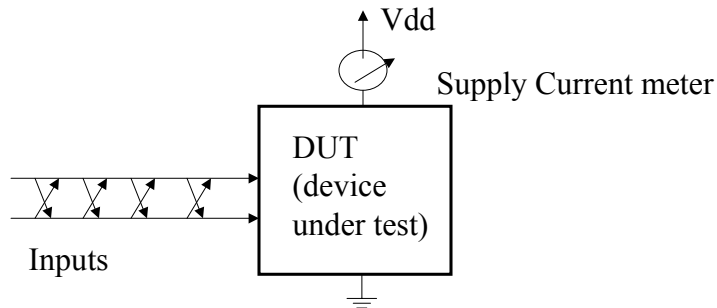
Static = proportional to number of transistors in system (will be a constant)

Dynamic = Capacitance switched at clock frequency (clock net, FF clock loads ) +

Capacitance switched at compute rates  
(combinational gates)

Not all combinational gates switch with each calculation. Their toggle rates are typically anywhere from 5% to 15% of the clock frequency. Logic synthesis techniques can be used to reduce the toggle rate of a system.

## Power Characterization



Change inputs at a known frequency with typical input sequence.  
 Measure Supply current. System Capacitance is:

$$P_d = V_{dd}^2 * C_{sys} * Freq$$

$$V_{dd} * I_{ss} = V_{dd}^2 * C_{sys} * Freq$$

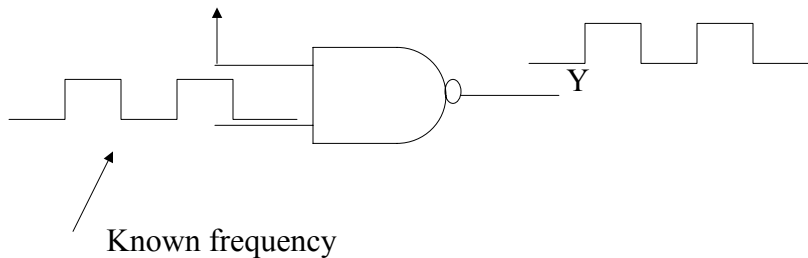
$$C_{sys} = I_{ss} / (V_{dd} * Freq)$$

System Capacitance for high performance microprocessors a few nano-Farads.

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## Gate Power Characterization



May have output of gate loaded by a typical FO4 load.

Measure  $I_{ss}$  for just the gate, compute effective switched capacitance of gate. Usually in the 10's to low 100's of femto-farads.

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## CMOS Technology Scaling

- See page 122-129 of Rabaey text
- Full Scaling –  $V_{dd}$  scaled by  $S$ , Dimensions by  $S$
- General Scaling -  $V_{dd}$  scaled by  $U$ , Dimensions by  $S$
- Fixed-Voltage Scaling - only Dimensions by  $S$
- Overall Capacitance scales by  $1/S$ , all scaling models
- Delay by  $1/S$  (short channel devices, all scaling models)