

EE 8273 Test #1 - Fall '03 – Reese

Student ID: _____ (no names please)

Work all problems. Closed book, closed notes, open calculator. When asked for explanations, be concise.

1. (6 pts) Show the transistor diagram for a STATIC CMOS, 2/1 mux that implements the equation “ $Y = AS' + BS$ ” (do not assume dual rail inputs). You do not have to show transistor sizes.
2. (4 pts) In the simple RC timing model we studied ($\text{Delay} = T_{\text{load}} + K \cdot C_{\text{load}}$), what does K physically represent in the circuit?
3. (8 pts) Assume you are characterizing a 2-input NAND gate using the simple RC timing model. How many spice measurements would you need to characterize ALL of the delays? Explain each measurement that you would make.

