

ECE 3724/CS 3124 Quiz #7 Reese Solution

Answer each of the following questions (you can use a calculator)

- a. (4 pts) Using `i2c_start`, `i2c_stop`, `i2c_putbyte()`, and `i2c_getbyte()` subroutines, write code that does a random address read from location 0xA0F0 in the serial EEPROM (515). Assume that both A0 and A1 of the EEPROM are tied high.

```
i2c_start();           //      UpperBlk A1  A0 Write
i2c_putbyte(0xAE);    // 1010   1      1   1   0
i2c_putbyte(0xA0);    // upper byte of address, could also be 0x20 as MSb is ignored
i2c_putbyte(0xF0);    // lower byte of address
i2c_start();           //      UpperBlk A1  A0 Read
i2c_putbyte(0xAF);    // 1010   1      1   1   1
i2c_getbyte();
i2c_stop();
```

- b. (1 pt) Given an input code of 0x45 to a 6-bit DAC with a 5V reference voltage, what is the output voltage?

By the formula:  $\text{input\_code} / 2^N * V_{\text{ref}} = 0x45 / 64 * 5 \text{ V}$   
 $= 69/64 * 5 \text{ V} = 5.39$ , which is greater than  $V_{\text{ref}}$ !!!! Impossible!

This was a mistake on my part – 0x45 is more than 6 bits!!!! Requires 7 bits.  
For a 7-bit DAC, would get  $69/128 * 5 \text{ V} = 2.69$

- c. (1 pt) Identify the bit and register in the I2C module of the PIC18 that is used to initiate a START condition.

Bit 0 of the SSPCON2 register

- d. (2 pts) Write C code that configures the A/D to use AN1 as an analog input,  $V_{\text{dd}}/V_{\text{ss}}$  as  $V_{\text{ref+}}/V_{\text{ref-}}$ , the conversion clock as  $F_{\text{osc}}/8$ , the A/D turned on, and a conversion NOT in progress.

```
ADCON1 = 0x00 (there are multiple solutions)
ADCON0 = 0x 49 = 01      001      0 0 1
                  Fosc/8  AN1          A/D on
```

- e. (1 pt) Why is every byte transmission on the I2C bus actually 9 bits? What does this provide?

Acknowledge bit, to ensure that the byte was received by an I2C device

- f. (1 pt) What is the fundamental difference between a successive approximation ADC and a flash ADC?

Speed – Successive approximation takes 1 clock per bit, Flash A/D takes 1 clock cycle (just a setting time of the comparators and combinational delay)