

ECE3424 Electronic Circuits Laboratory

Experiment #10

Mixed applications using both JFETs and BJTs

vers 2.3

OBJECTIVE: Measure properties and limitations of special purpose circuits that take advantage of the properties of both JFETs and BJTs.

Comment and Exposition: Both the JFET and the BJT are junction devices, and as such are able to survive considerable abuse as well as handle larger power levels. In spite of their differences, it is natural that they be regarded as devices of similar disposition. The characteristics of one are often of application benefit to the other.

1. Because of the parabolic character of the FET model, it finds a role as a linear voltage-controlled conductance. At low V_{DS} (for which $I_D(V_{DS})$ is parabolic) the ratio I_D/V_{DS} will be

$$\frac{I_D}{V_{DS}} = \beta \left[(V_{GS} - V_P)V_{DS} - \frac{1}{2}V_{DS}^2 \right] / V_{DS} = \beta \left[(V_{GS} - V_P) - \frac{1}{2}V_{DS} \right] \quad (10-1)$$

I_D/V_{DS} is the static conductance. If the FET (JFET) is configured as shown by figure 10-1a it becomes a linear conductance, as reflected by the simulation (figure 10-1b)

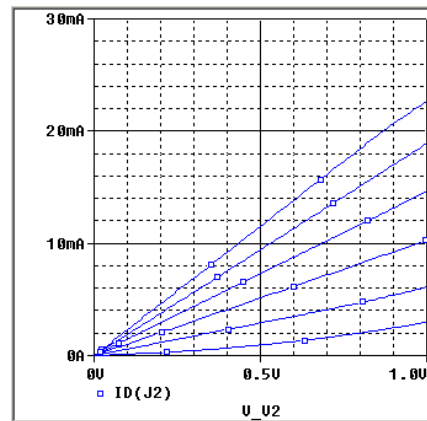
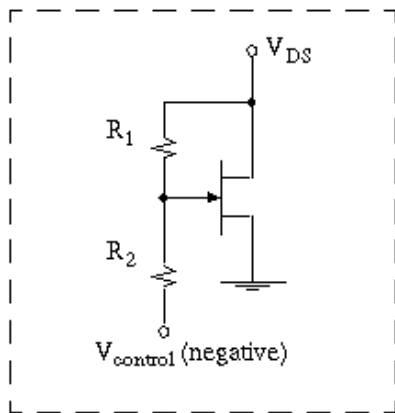


Figure 10-1(a). Linearizing topology for the FET static conductance (low V_{DS}).

Figure 10-1(b). Simulation of I vs V response of figure 10-1b.

The $R_1 = R_2$ voltage divider adds a voltage of $0.5V_{DS}$ to V_{GS} and equation (10-1) will then become

$$G_{DS} = \frac{I_D}{V_{DS}} = \beta \left[(V_{GS} + 0.5V_{DS} - V_P) - \frac{1}{2}V_{DS} \right] = \beta(V_{GS} - V_P) \quad (10-2)$$

and the value of G_{DS} is controlled by V_{GS} .

2. The JFET also can take on the role as a high input impedance device for which very high circuit R_{in} can be achieved, as is represented by the voltage follower circuit of figure 10-2. But it usually lacks the high transconductance characteristics of the BJT, which are key to forming a good buffer circuit. The circuit of figure 10-2 uses both of these devices to achieve a nearly ideal unity-gain buffer, which has natural applications for almost every gain circuit in existence.

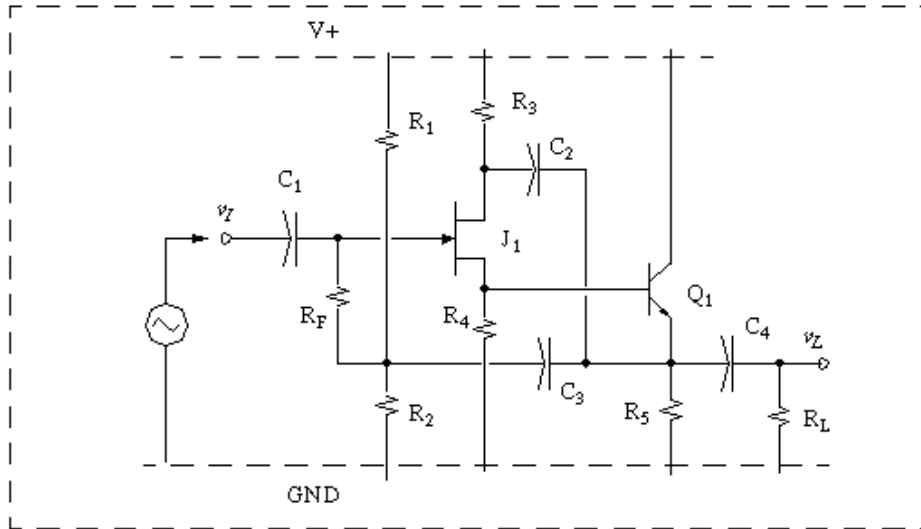


Figure 10-2: High input impedance voltage follower

For the circuit of figure 10-2 circuit input impedances on the order of $100\text{M}\Omega$ are not unreasonable. This type of circuit is therefore often suggested for such extreme instruments as an electrometer, for which even the leakage of individual electrons is to be avoided.

The circuit achieves its high input impedance through (1) the high input impedance of the reverse-biased junction of the jFET and (2) the (feedback through C_3) multiplying effect on the feedback resistance R_F for which

$$R'_F = R_F / (1 - v_L/v_I) \quad (10-4)$$

which is very high since v_L/v_I is close to unity for a BJT-driven voltage follower.

PROCEDURE:

A-1. The transistors for mixed device applications are the 2n3904 (BJT) and the 2n5457 (JFET) as well as the opamps, and should be in your parts kit. The purpose of the exercise will be to evaluate the application circuits that have been identified and confirm their functionality.

The test circuit for the linearized JFET topology is that of figure 10A-1 and is used to control a signal transfer opamp. Transfer gain of the signal opamp is $1 + G_{DS}/G_2$, for which $R_2 = 1.0k\Omega$ for the test circuit and G_{DS} is given by equation (10-2). Since the JFET is in series with capacitance C_N its V_{DS} will be very nearly zero and its G_{DS} conductance will be almost identical to equation (10-2).

The bias opamp for the FET is configured in the inverting configuration. By superposition inputs V_B and V_A will apply a $V(\text{control}) = V_C$ to the FET topology of

$$V_C = -(V_B/8 + V_S(t)) \tag{10-5}$$

for which $V_G = 0.5V_C$. V_B is either used to bias the FET into a conducting mode or to control transfer gain. $V_S(t)$ is a modulation signal. Since modulation $V_S(t)$ is expected to be at a much lower frequency than $V_I(t)$, coupling capacitance C_N must be large ($10\mu\text{F}$).

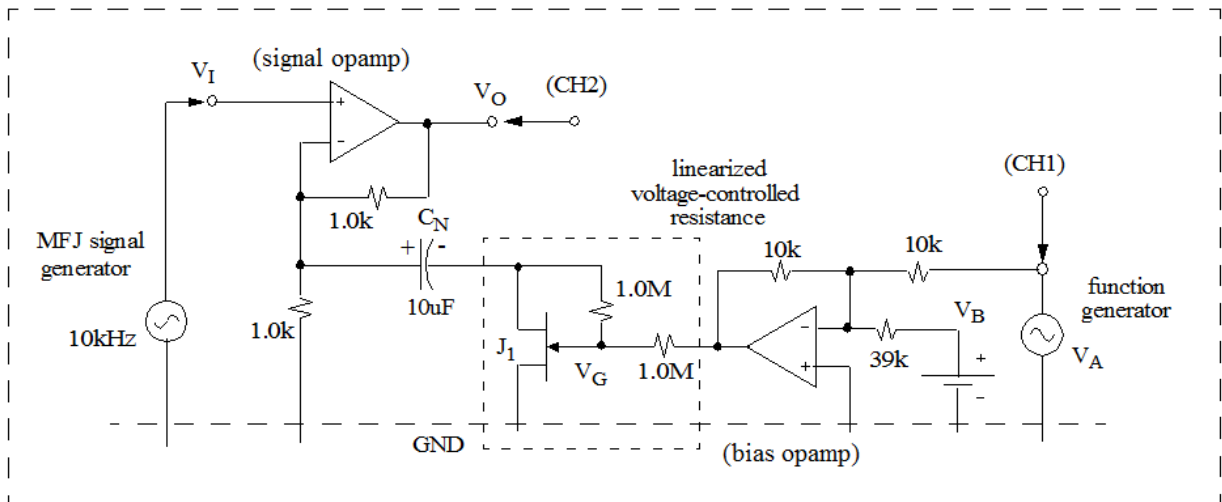


Figure 10A-1. Linearized voltage-controlled amplifier topology. In this case it is used as a mixer, for which the gain (and amplitude) of output signal at V_O is controlled by amplitude modulation signal at V_A .

A-2. Construct the circuit of figure 10A-1 on your prototyping board. Placement and wiring suggestions are given by photo figure 10A-2a, but most of the art is left to you.

Voltage V_B is taken from the bench power supply. Let V_I be a 200mV pk-pk, 10kHz signal from the built-in signal generator of the MFJ box. CH2 and CH1 of the O-scope should be connected as indicated, but with CH1 ignored at the outset. Capacitance $C_N = 10\mu\text{F}$ electrolytic with polarity as indicated by figure 10A-2.

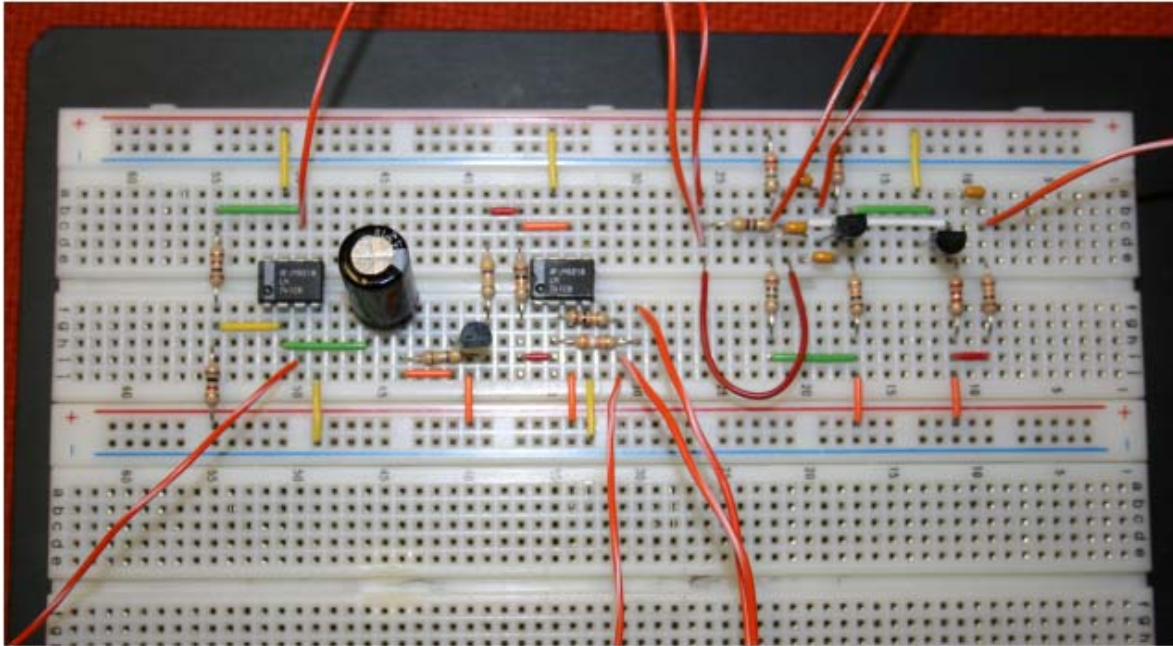


Figure 10A-2a Placement and wiring for figure 10A-1

Figure 10A-2b. Placement and wiring for figure 10B-1

A-3. Set V_B to 8V. Set the waveform generator in the triangular wave mode at 200Hz and amplitude $V_a = 1.0V$. The output waveform at V_O should show a triangular modulation similar to that of figure 10A-3 that correlates with the triangular waveform at CH1, from which you should be able to take measurements of the circuit gain A_V vs $V_B + V_a(t)$. Enter this information into the data table. In your analysis you will extract a slope coefficient of A_V vs V_B . In your analysis you should find that A_V vs $(V_B/16)$ should be reasonable close to the value of the jFET conduction coefficient β .

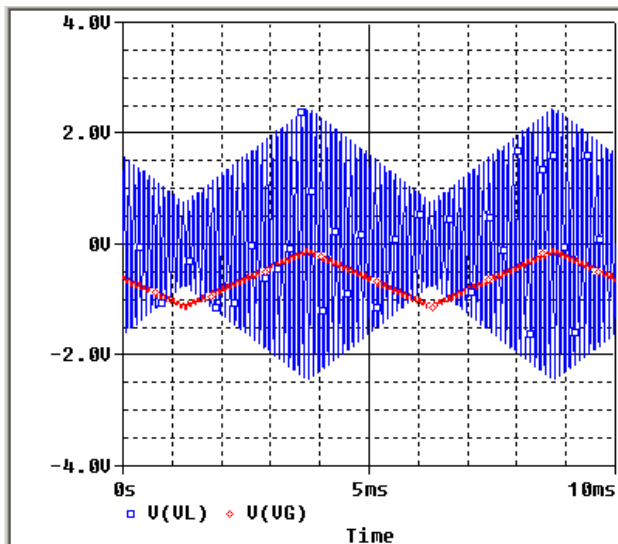


Figure 10A-3: Simulation of circuit: Circuit gain at V_O linearly controlled by V_G

B-1. The high input impedance topology will have input impedance that relates as much to feedback across R_F as to the high input impedance characteristics of the JFET, for which equation (10-4) describes the outcome. The bench topology that we will use is shown by figure 10B-1.

Construct the circuit of figure 10B-1 on your prototyping board. The 12-V supply is that of the MFJ box. Input is a 10kHz, 1.0V input source. Placement and wiring suggestions are given by photo figure 10A-2b, but most of the art is left to you.

You should check the value of the 4.7Meg source resistance using your DMM before inserting it into the prototyping board since it is your 'reference' resistance for assessment of input resistance R_{in} .

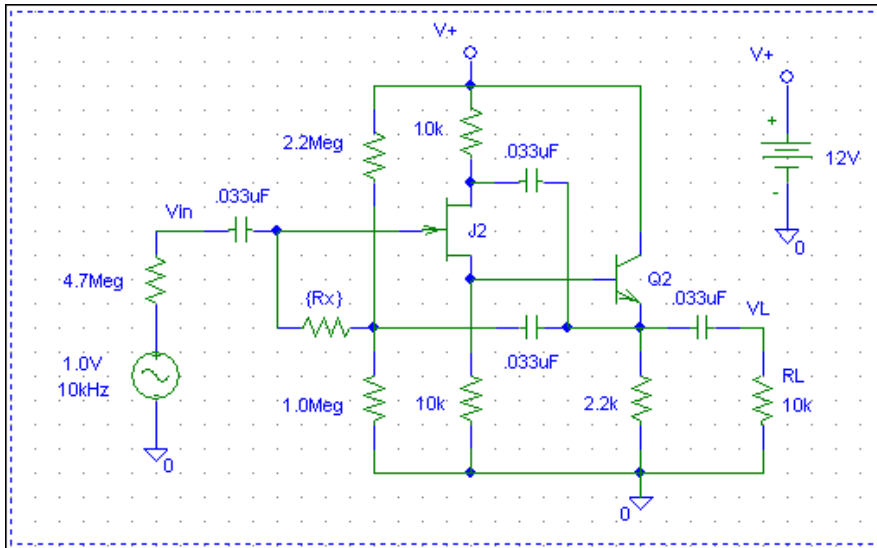


Figure 10B-1: High input impedance topology. R_x = Resistance box

B-2. The test configuration for measurement of R_{in} is shown by figure 10B-2 and is the same as used in an earlier experiment, as is the measurement technique. R_S corresponds to the 4.7M Ω resistance.

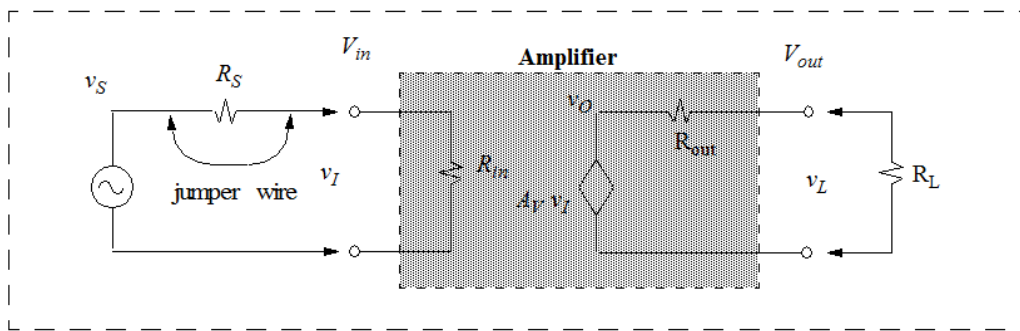


Figure 10B-2. Measurement of input resistance.

Measurement is accomplished by the ON/OFF application of the jumper wire, for which the voltage-divider at the input gives

$$\frac{v_I}{v_S} = \frac{R_{in}}{R_{in} + R_S} \quad (10-3a)$$

where v_I = value of input level with jumper wire disconnected (OFF). The measurement is more easily accomplished by tracking the effect at the output, for which

$$\frac{v_{L2}}{v_{L1}} = \frac{R_{in}}{R_{in} + R_S} \quad (10-3b)$$

for which v_{L1} = value of output level with jumper wire ON, v_{L2} is with it OFF. Input resistance of the amplifier is determined by solving equation (10-3b) for R_{in} .

Set the initial value of your resistance box (R_x) to 10k Ω . Connect CH1 to V_{in} and CH2 to V_L . Determine pk-pk amplitude of both with and without the jumper wire connected. The 'measure' button on your O-scope will give the pk-pk values for the input channels. Add values to a new data table from which you will eventually (use Excel to) extract input resistance R_{in} .

B-3. Repeat part B-2 for $R_x = 20\text{k}\Omega, 40\text{k}\Omega, 80\text{k}\Omega, 100\text{k}\Omega, 200\text{k}\Omega, 400\text{k}\Omega, 800\text{k}\Omega, 1\text{M}\Omega, 2\text{M}\Omega, 4\text{M}\Omega,$ and $8\text{M}\Omega$. These are approximately at 'octave' increments. Some of the measurements at the upper limit may be more challenging, so include a measurement accuracy.

ANALYSIS and REPORT:

1. Create a column that show the theoretical value of G_{DS} (equation 10-2) for estimated values of β and V_P , even though you could probably look these values up on the specification for transistor 2n5457. Create a second column that gives gain v_L/v_I as given by equation (10-4) and component values as used by your test circuit.
2. Compare the equations with a plot of your data and (10-4) vs V_G (or $V_B/16$) and adjust the values of β and V_P until you get a reasonable fit.
3. Execute a simulation of the circuit of figure 10A-2 in pspice, but step V_B using the **Analysis>Setup>Parameter** menu. In order to acquire a plot of gain vs V_B , use the 'Trace >Performance Analysis' menu of your Probe postprocessor and have it perform the function

$$\text{Max}(\text{abs}(V(\text{Vo})/50\text{mV}))$$

which should yield a plot of signal gain $|v_L/v_I|$ vs V_B . Make comparison of this plot to those developed under part 3.

4. Using the data of parts B-2 and B-3 (use Excel to) determine the input resistance R_{in} of the circuit via the voltage divider with $R_S = 4.7\text{Meg}$. Make a plot of R_{in} (as measured by this process) vs R_X . Scale for log-log display.
5. Execute a circuit simulation of figure 10B-1, with R_X stepped using the **Analysis>Setup>Parameter** menu. Use the 'Trace >Performance Analysis' menu of your Probe postprocessor and have it perform the function

$$4.7\text{Meg}/((\text{Max}(V(\text{Vs}))/\text{Max}(V(\text{Vin}))) - 1)$$

where V_{in} and V_S are as indicated by the figure 10B-1. This performance analysis should give a simulation result for R_{in} vs R_X similar to that shown by figure 10B-1R. Make use of log-log scaling since it is more consistent with the octave measurement scheme of parts B-2 and B-3.

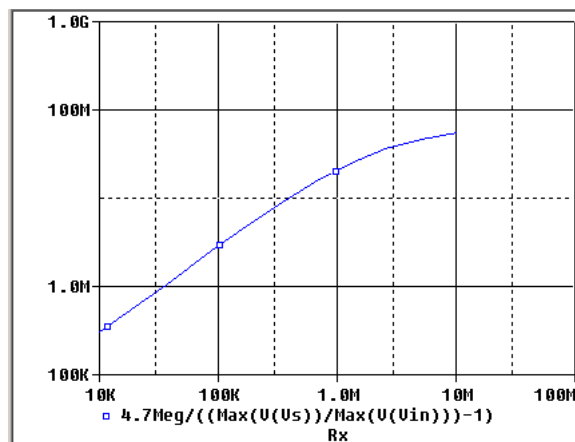


Figure 10B-1R: Simulation of figure 10B-1. Log-log scaling can be accomplished by toggling the axis displays (buttons) on your Probe window.

Compare this simulation result to a plot of your measurements of R_{in} vs R_X , which should also use a log-log display.

APPENDICES

APPENDIX A-1. Transistors

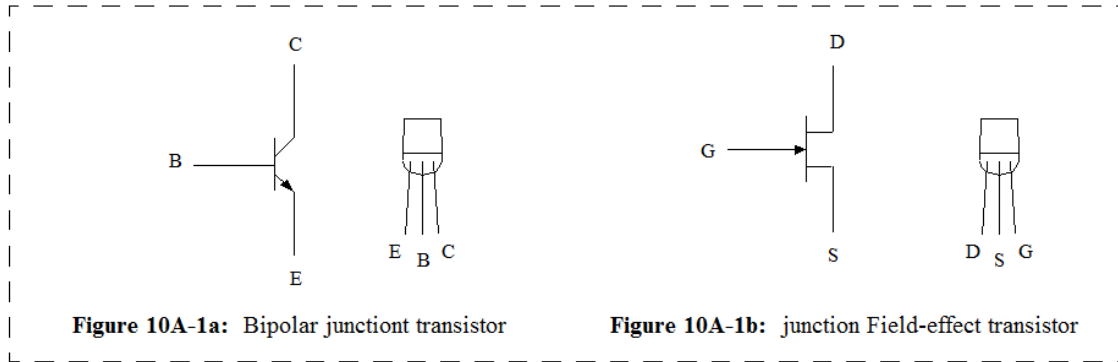


Figure 10A-1a: Bipolar junction transistor

Figure 10A-1b: junction Field-effect transistor

APPENDIX A-2. Pin-out for 741C opamp

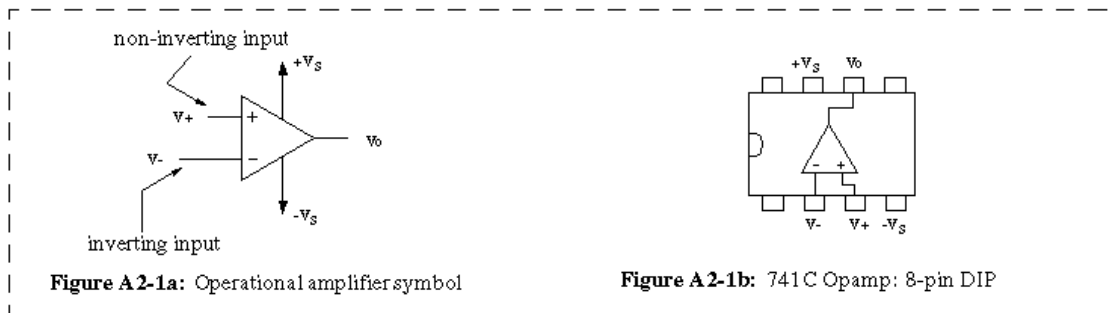


Figure A2-1a: Operational amplifier symbol

Figure A2-1b: 741C Opamp: 8-pin DIP

APPENDIX A-3. Extra diode and capacitance parts. You should have a sufficient number in your parts kit, but if not some extras may be located in the parts box in the parts/wires drawer of your workstation.

