

ECE3424 Electronic Circuits Laboratory

Experiment #11 Measurement of parasitic capacitances of BJTs and FETs vers 2.12

OBJECTIVE: Measure parasitic capacitances of the Q2n3904 and the J2n5457 transistors

Comment: The speed of a transfer circuit is synonymous with its frequency and noise profiles. These profiles are dependent on (1) bias frame and (2) parasitic capacitances of the transistors and the wiring.

For the BJT the parasitic capacitances are represented figure 11-1(a). For the FET the parasitic capacitances are represented by figure 11-1(b). These small capacitances are primarily due to junction capacitance. For most transistors they are on the order of pF. Large power-transistor cousins may have parasitic capacitances on the order of nF.

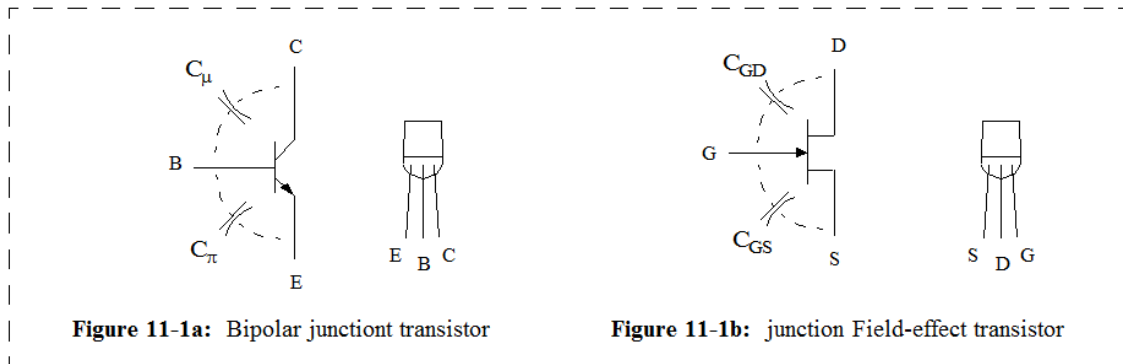


Figure 11-1. Parasitic capacitances of the BJT and FET

As shown by figure 11-1, parasitic capacitances of the BJT are called C_μ and C_π . The base-collector capacitance, C_μ is almost entirely a junction capacitance

$$C_\mu = C_{JC} \quad (11-1a)$$

Base-emitter capacitance C_π consists of both a junction capacitance and a diffusion capacitance $C_D = g_m \tau_F$.

$$C_\pi = C_{JE} + g_m \times \tau_F \quad (11-1b)$$

where g_m is the transconductance and τ_F is the forward transit time of the device.

For the jFET both of the capacitances are junction capacitances.

$$C_{GS} = C_J(GS) \quad (11-2a)$$

$$C_{GD} = C_J(GD) \quad (11-2b)$$

The speed of the circuit is defined by these small parasitic capacitances. Speed manifests itself in the frequency domain by a high-frequency roll-off at f_{3dB} . The object of this lab exercise is to undertake a series of measurements of the upper frequency corner and use them to extract parasitic capacitance parameters of these transistors.

PROCEDURE:

A-1. The simplest topology for probing transistor parasitic capacitances is shown by figure 11A-1. In this figure it is used to probe a 2n3904 BJT, same as was used in previous experiments. You will need two of these transistors and you will need to leave adjacent space on your protoboard for both. The upper and lower voltage rails (+12V and GND) are available on your MFJ box.

Take note that when both jumper wires are disconnected the v_C/v_B gain = -1.0V/V. When jumper wire #1 is connected as shown (and jumper wire #2 disconnected) the v_C/v_B gain = -2.0V/V. The effective capacitance between B and C is enhanced by v_C/v_B according to

$$C'_{BC} = C_{BC}(1 - v_C/v_B) \tag{11-3}$$

and this effect is employed to discriminate and identify the parasitic capacitance C_{BC} .

For snake check of the circuit let the input signal be set to 20kHz at 1.0V pk-pk amplitude. The amplitude is arbitrary but should be kept fairly low in order to minimize distortion at the output.

The jumper wires are a convenience for invoking a set of options that will help to discriminate one parasitic capacitance from another. The R_{box} is needed to discriminate resistance contributions. Transistor capacitances are typically pF in magnitude. Parasitic capacitance between rows of the protoboard are also on the order of pF, and must be screened by the measurement sequence.

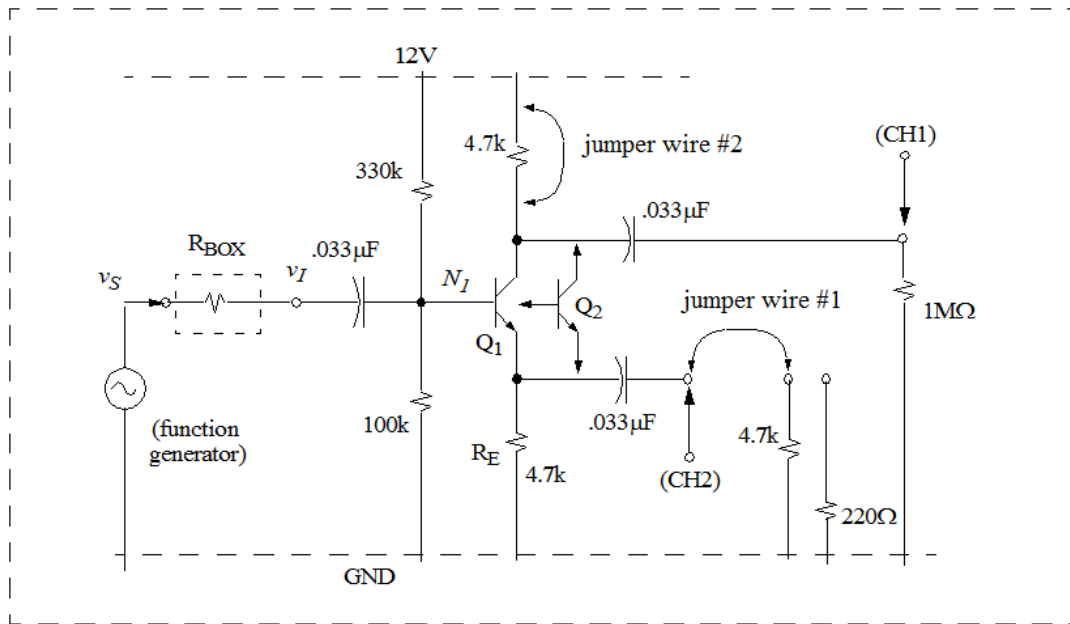


Figure 11A-1: Test bed for extraction of parasitic BJT capacitances

A-2. Set up the circuit of figure 11A-1 on the protoboard. Figures 11A-2a and 11A-2b should help with placement and wiring. Transistor leads are identified by figure 11-1. The initial setting of the resistance box should be set at 25kΩ

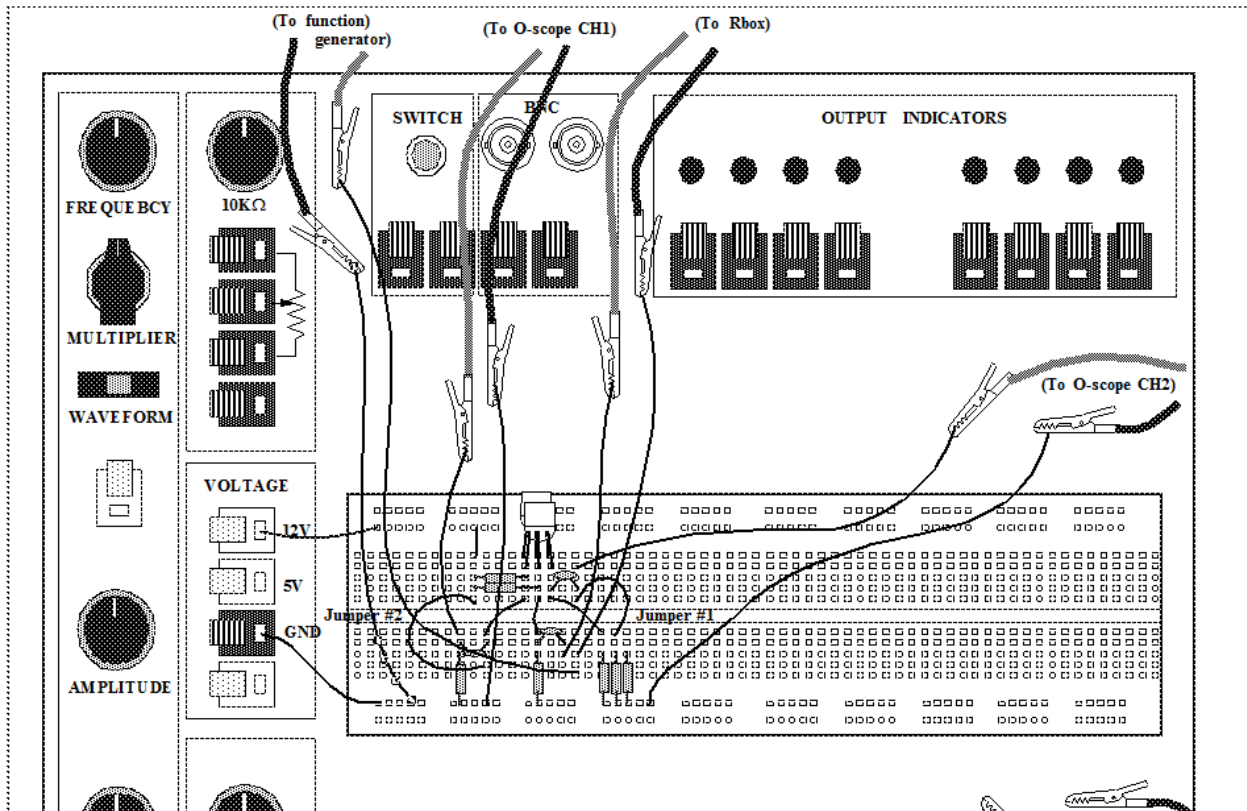


Figure 11A-2a. Placement and wiring suggestions. Wires spread to reduce parasitic wiring capacitances of the protoboard.

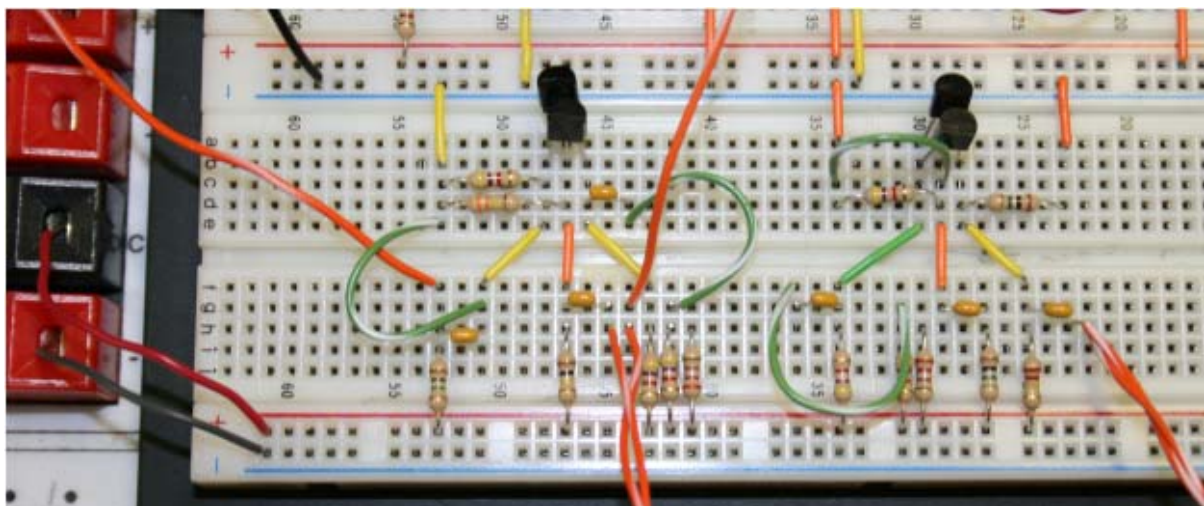


Figure 11A-2b. Placement and wiring photo, circuits of figures 11A-1 and 11C-1. Both jumper wires are shown connected, even though not inclusive all of the tests. Wires should be somewhat spread in order to reduce parasitic capacitance contributions from the protoboard.

A-3. With both of the jumper wires disconnected, monitor the output at CH1. Ignore CH2. You must be at a workstation that has variable sweep and capability to at least 2MHz. Sweep the frequency by hand. Identify the mid-band signal amplitude and then increase frequency until the amplitude rolls off to approximately 70% of the mid-band value. The 70% level corresponds to the f_{3dB} point. Determine it as accurately as possible. Expect f_{3dB} on the order of 500kHz to 2MHz (you need a signal generator that can reach this range). If f_{3dB} is out of range of the signal generator move on to part A-4, which will offer lower frequencies.

A-4. Repeat part A-3, but with $R_{box} = 50k, 100k, 200k$ and $400k$. For each of these resistances you should see successively lower values of the 3dB roll-off corner. The set of f_{3dB} data points (including that of part A-3) must be sufficient for you to determine a capacitance value by means of f_{3dB} vs conductance plot like that of (the simulation) figure 11A-4. They should be entered in Excel as a column of 5 data points (or fewer if some of the data points are out of reach). You must acquire enough data points to extract slope $\Delta f_{3dB} / \Delta G_{box}$ to reasonable accuracy. The slopes correspond to $(1/C)$ values. Adjust amplitude of the source as needed for each value of R_{box} such that the distortion at V_{out} is avoided and such that reasonably good measurements of f_{3dB} are accomplished.

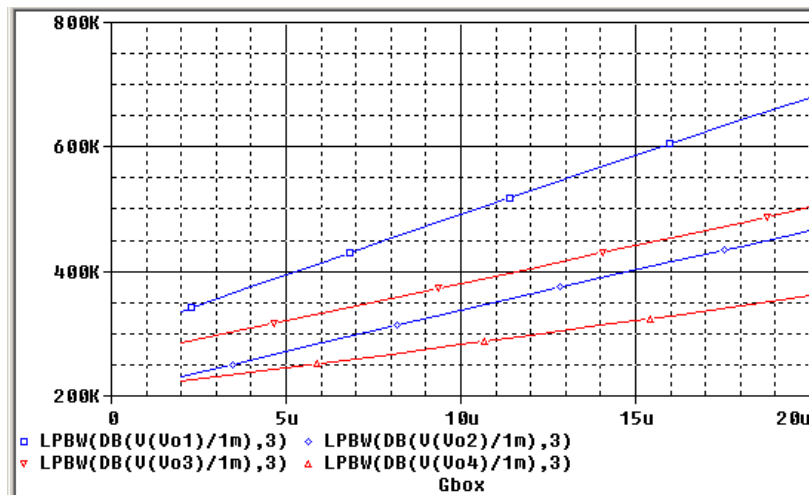


Figure 11A-4. Simulation of tests using pSPICE. Note that the plot is f_{3dB} vs ($G_{box} = 1/R_{box}$)

A-5. Insert an extra transistor (Q2) in parallel with Q1. Repeat part A-3 and A-4 and generate a 2nd column (set) of f_{3dB} data points.

A-6. Remove the extra transistor Q2. Insert jumper wire #1 to emplace a second 4.7k resistance in parallel with R_E though the .033uF capacitance. Repeat parts A-3 and A-4 for a 3rd column (set) of f_{3dB} data points.

A-7. Restore the second transistor Q2 to part A-6 keeping jumper wire #1 in place. Repeat the measurement sequence for the R_{box} to generate a 4th column set of (5) f_{3dB} data points.

B-1. Remove transistor Q2. Insert jumper wire #1. Keep jumper wire #2 (as connected to the 4.7k resistance) in place. Monitor CH2 and ignore CH1. Repeat the measurement sequence with R_{box} stepped from 25k to 400k as before to generate a new column set of (5) f_{3dB} data points. Caution: This is a relatively high frequency circuit and may be partly out of bounds of your instrumentation, so it is possible that you will not be able to acquire a good set of points. Try to acquire at least three data points in order to define a slope. The simulation of this set of measurements is reflected by figure 11B-1.

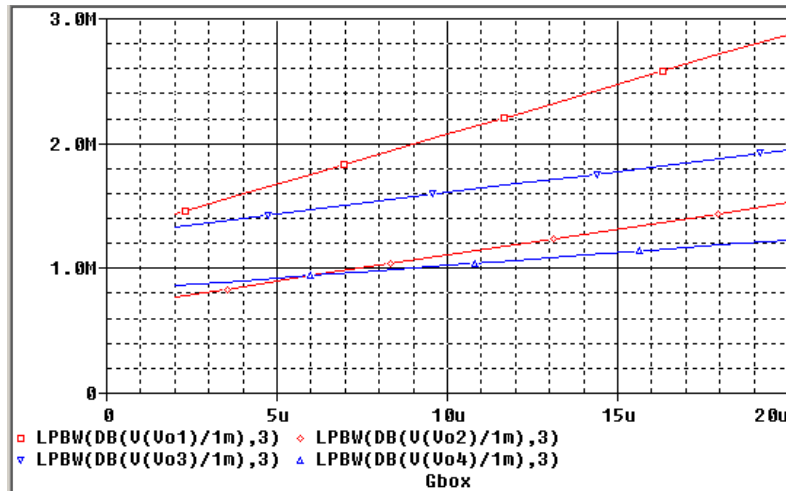


Figure 11B-1. Simulation of emitter tests using pSPICE. f_{3dB} vs $1/R_{box}$.

B-2. Add transistor Q2 to part B-1 and repeat the measurement sequence for a 2nd set of data points. This set (column) of data points should be a little more tractable than part B-1.

B-3. Remove transistor Q2 to part B-1 and move jumper wire #1 so that the 220 Ω resistance is inserted in place of the 4.7k resistance. Repeat the measurement sequence for 3rd column set of f_{3dB} data points.

B-4. Add transistor Q2 to part B-3 and repeat the measurement sequence for a 4th column of f_{3dB} data points.

C-1: Replace the circuit topology of figure 11A-1 with that shown by figure 11C-1. Repeat the measurement sequence of part A, except this time using a pair of nJFETs as shown

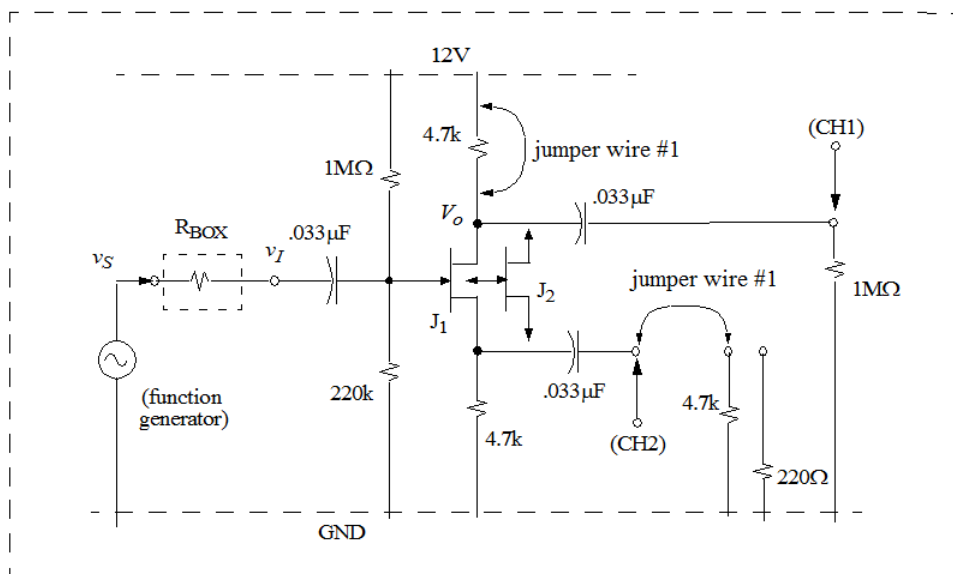


Figure 11C-1. Test bed for extraction of JFET parasitics

D-1 Repeat the measurement sequence of part B, except with figure 11C-1 and the pair of nJFETs rather than the BJTs.

ANALYSIS and REPORT:

1. Plot the data of parts A-3 through A-7 (four columns) vs $I/Rbox$ as the first column (X-axis) using the X-Y plot function of Excel. The four plots are f_{3bD} vs $Gbox$ and should resemble those of figure 11A-4 even though it is a simulation.

Extract the slope for each trace (even if only rough). The slopes correspond to (I/C) values. Keep track of units. List the four capacitance values that you extract in the order C_1, C_2, C_3, C_4 corresponding to the order of the extracted data. Each corresponds to different circumstances of Miller effect and capacitance pairing. Parasitic wiring capacitances (C_W) are not paired but are subject to the Miller effect.

The Miller voltage multiplication effect is $C'_{BC} = C_{BC}(1 - v_C/v_B)$. For the circuit of part A the Miller voltage multiplication effect at the emitter will diminish the effect of C_{BE} since v_E/v_B is approximately 1.0.

The 1st and 2nd data sets have a $v_C/v_B = -1$. The 2nd and 4th data sets have 2x transistor contributions. The 3rd and 4th data sets have $v_C/v_B = -2$. An unknown wiring capacitance C_W exists between B-C and between B-E and another unknown parasitic wiring contribution C_{WN} is at node N.

Confirm the following relationships:

$$C_1 = 2(C_{JC} + C_W) + C_{WN} + C_{BE}^1 \quad (11-4a)$$

$$C_2 = 2(2C_{JC} + C_W) + C_{WN} + C_{BE}^2 \quad (11-4b)$$

$$C_3 = 3(C_{JC} + C_W) + C_{WN} + C_{BE}^1 \quad (11-4c)$$

$$C_4 = 3(2C_{JC} + C_W) + C_{WN} + C_{BE}^2 \quad (11-4d)$$

The superscript K reflects the transistor count. Emitter capacitances $C_{BE}^K = \alpha_K (K \times C_{JE} + C_W + g_m \tau_F)$ are expected to be small since voltage multiplication coefficient $\alpha_K = (1 - v_E/v_B)$ is approximately .012 and .024, respectively. Use Excel to solve for the best fit values for the unknown parasitic capacitances C_{JC} , C_W , and C_{WN} and highlight them as outcome values.

2. Repeat part 1 except for the four datasets generated by part B.

The four capacitances at node N will see no Miller effect between B-C and a noticeable Miller effect between B-E only for the 3rd and 4th datasets. The 2nd and 4th data sets have 2x transistor contributions as represented by superscript K .

3. Using the data of parts 1 and 2 identify the best fit values of C_{JC} , C_{JE} , and τ_F for the 2n3904 transistor. Parasitic wiring effects C_W exist between B and C and between B and E, and an unknown parasitic wiring contribution C_{WN} will exist at node N. Once again there will be four equations.

$$C_1 = C_{JC} + C_W + C_{WN} + C_{BE}^{11} \quad (11-4a)$$

$$C_2 = 2C_{JC} + C_W + C_{WN} + C_{BE}^{12} \quad (11-4b)$$

$$C_3 = C_{JC} + C_W + C_{WN} + C_{BE}^{12} \quad (11-4c)$$

$$C_4 = 2C_{JC} + C_W + C_{WN} + C_{BE}^{22} \quad (11-4d)$$

where $C_{BE}^{KN} = \alpha_N (K \times C_{JE} + C_W + g_m \tau_F)$, where K = number of transistors. Emitter voltage multiplication coefficients $\alpha_1 \sim .024$ for the 1st and 2nd datasets and $\alpha_2 \sim 0.22$ for the 3rd and 4th datasets. Transconductance $g_m \sim 16\text{mA/V}$. (Note $\alpha_K = (1 - v_E/v_B)$, same as before but v_E/v_B is smaller.)

Using Excel and the results of part 1 solve for the best fit values for the unknown parasitic capacitances C_{JE} and τ_F and highlight them as outcome values.

The capacitance C_{JC} that you measure should differ from that for the model parameter C_{JC} by approximately a factor of two due to the reverse bias on the BC junction.

3. Repeat part 1 except for the FET. Resolve values of C_{JD} , C_W , C_{WN} from these measurements.

4. Repeat part 2 except for the FET. Resolve values of C_{JS} , C_W , C_{WN} from these measurements. The process is the same as for the BJT except that $\tau_F = 0$. Since g_m is much smaller for the jFET, $\alpha_2 \sim 0.6$.

The capacitance C_{JD} that you measure should differ from that for the model parameter C_{JD} by approximately a factor of two due to the reverse bias on the gate-drain junction.

5. Execute a pSPICE on the circuit of figure 11A-1 with an input VAC source at 1mV and the CH1 output node labeled as *Vo1*. Let $G_{box} = 1/R_{box}$ be varied by means of the **Analysis>Setup>Parameter** menu. Under the postprocessor (Probe) menu invoke the 'Performance Analysis' menu and execute the following function

LPBW(V(Vo1)/1mV,3) {or for later versions: Cutoff_Lowpass_3dB(V(Vo1)/1mV) }

Invoke the same simulation for all four options of transistor pairing and jumper wires (four different schematics but same source and a separate $R_s = \{1/G_{box}\}$ for each. Be economical about components or you will exceed the parts/page limit. Overlay all four traces. Your result should not be unlike that of figure 11A-4.

6. Execute a pSPICE on the circuit of figure 11C-1 with the input source at 1mV and the output node labeled as *Vo1*. Let $G_{box} = 1/R_{box}$ be varied by means of the **Analysis>Setup>Parameter** menu. Under the postprocessor (Probe) menu invoke the 'Performance Analysis' menu and execute the following function

LPBW(V(Vo1)/1mV,3) {or: Cutoff_Lowpass_3dB(V(Vo1)/1mV) }

Execute the simulation for all four options of transistor pairing and jumper wires (four different schematics but same source). Be economical about components or you will exceed the parts/page limit. Overlay all four traces.