

ECE3424 Electronic Circuits Laboratory

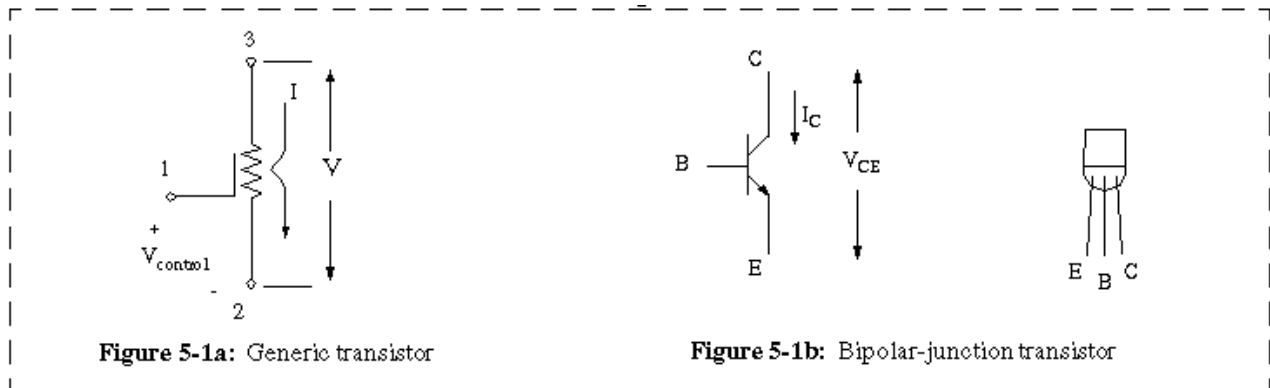
Experiment #5

I-V Characteristics of the Bipolar-junction transistor

vers 1.8

OBJECTIVE: Assess the output I-V characteristics of the Bipolar-Junction Transistor (BJT) and evaluate behavior of the forward current gain β_F and Early voltage V_A device parameters.

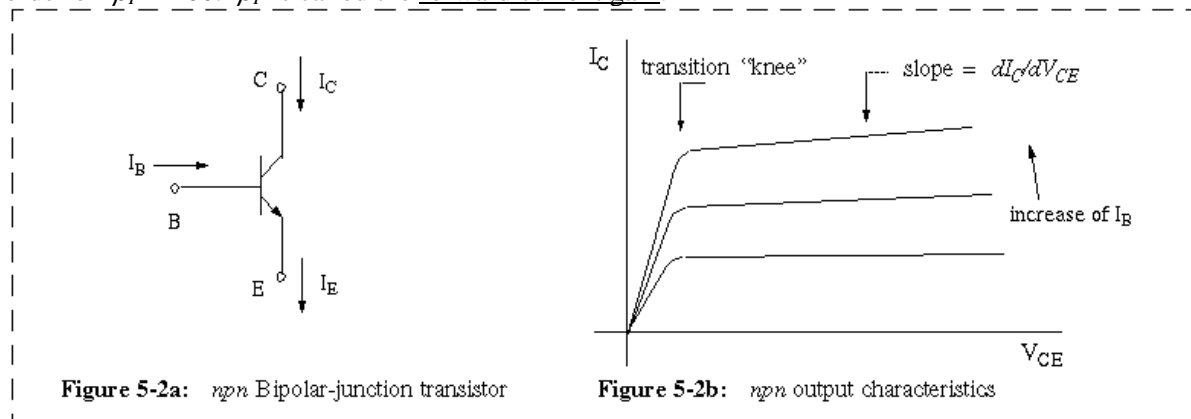
Comments: Transistors, regardless of type, are represented as a 3-terminal device. The transistor is effectively an input-controlled conductance, as represented by figure 5-1a. There are two basic types of transistor (1) the BJT and (2) the FET. Individually packaged transistors are usually BJTs. The symbol for the BJT and its typical package are represented by figure 5-1b.



For the BJT, output characteristics are usually specified in terms of I_C vs V_{CE} , as indicated by figure 5-2b, as if it were a simple conductance like the generic transistor device of figure 5-1a.

The BJT is a construct of two *pn* junctions back-to-back (hence the name bipolar-junction device). Therefore the control terminal also draws current, as represented by figure 5-2a.

The control terminal, which is called the Base, draws a small current I_B on the order of μA . Magnitude of the output current I_C is proportional to I_B , and usually is on the order of mA. The output characteristics of the BJT are typically of the form as represented by figure 2-2b. The ratio of I_C to I_B is on typically on the order of $\beta_F = 100$. β_F is called the forward current gain.



Note that $I_E = I_B + I_C$. But, since $I_B \ll I_C$, we sometimes say that I_C and I_E are approximately equal.

Your task is to measure the device characteristics of the BJT. The specific transistors to be evaluated are:

2n3904 (*npn* transistor)

2n3906 (*pnp* transistor)

PROCEDURE:

The test circuit for extracting the characteristics of an *npn* (2n3904) bipolar-junction transistor is shown by figure 5A-1. A large-amplitude triangular-wave signal is applied across the transistor by the signal generator. Diode D1 is oriented so that the negative swing of the signal across the transistor will be suppressed. Current through the transistor is measured by opamp circuit and the voltage across R_X . Current into the base of the transistor is defined by resistance R_{BB} and by external variable power supply V_{BB} . Diode D1 is oriented so that the negative swing of the AC signal across the transistor is suppressed.

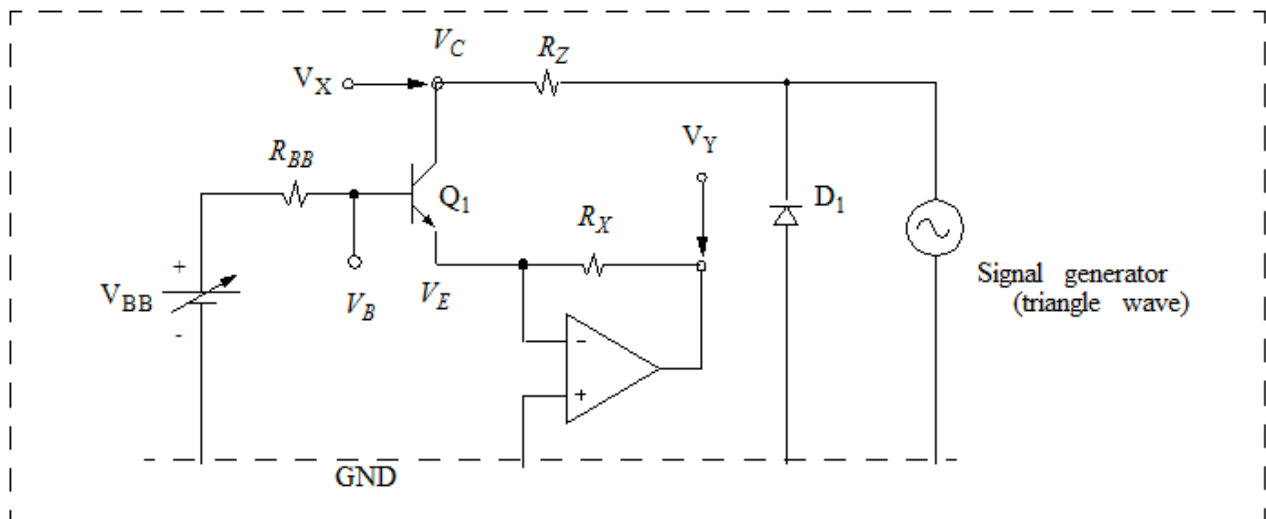


Figure 5A-1. Test frame for measurement of *npn* BJT characteristics. CH-1 should be connected to V_X and CH-2 should be connected to V_Y .

A-1. Set up the circuit of figure 5A-1 on the prototyping motherboard with $V_{BB} = 0$ VDC and the amplitude of the signal generator reduced to zero. Choose voltage rails for the opamp as ± 12 V and GND as provided by the MFJ prototyping box. Q1 is the 2n3904 which is an *npn* high speed switching transistor. For the first set of tests $R_{BB} = 100\text{k}\Omega$, $R_X = 1\text{k}\Omega$ and $R_Z = 100\Omega$. Figures 5A-2a and 5A-2b should give you some suggestions for placement and wiring.

The opamp serves the purpose of forcing the emitter voltage V_E to virtual ground as well as providing a means to measure output current through the transistor. It has the disadvantage of inverting measurement voltage V_Y , which therefore will display the I-V representation of the BJT upside down from that represented by figure 5-2b. Other than being inconvenient it will not otherwise compromise the measurement and data extraction process.

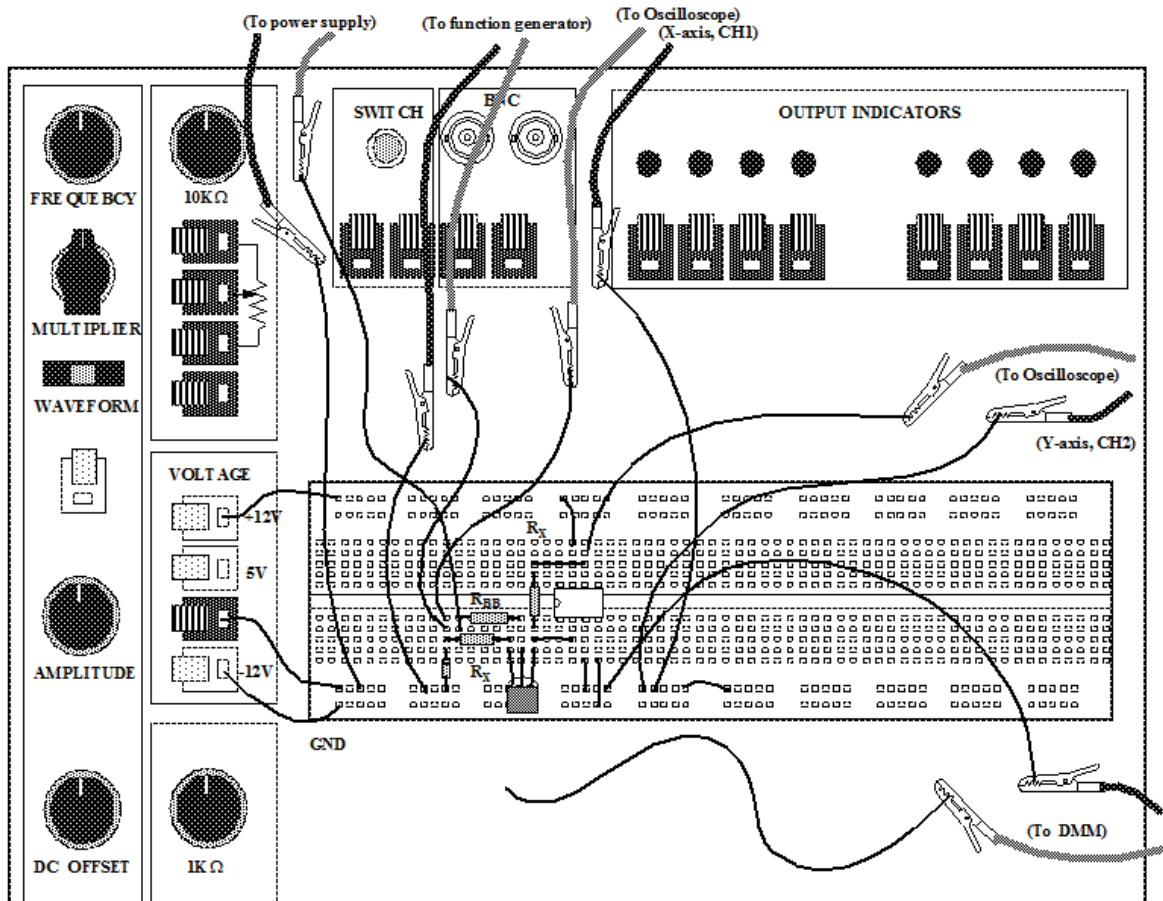


Figure 5A-2a. Suggestions for placement and wiring of the test circuit.

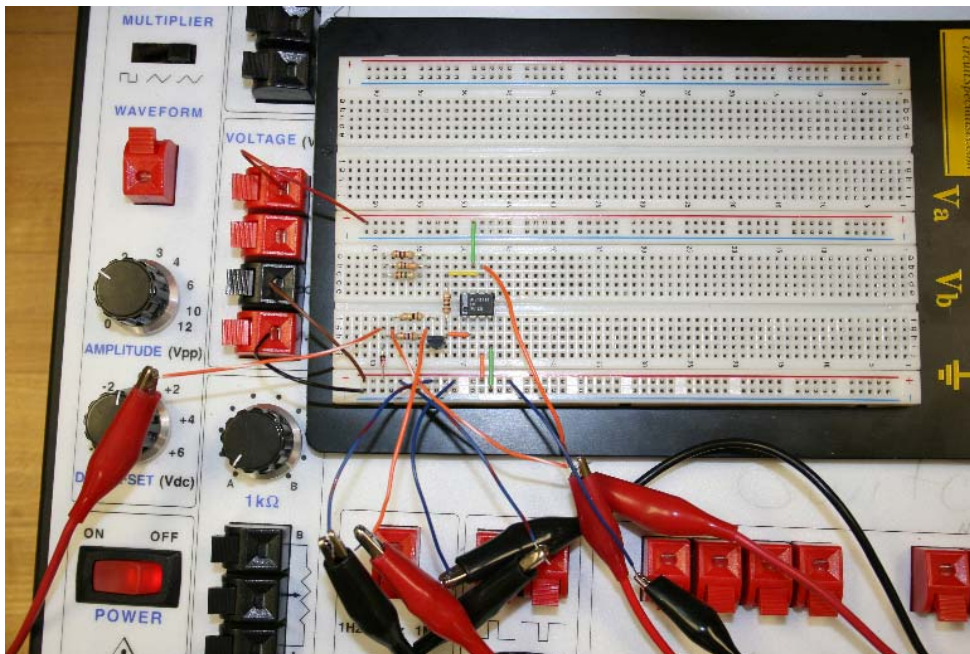


Figure 5A-2b. Photo of placement and wiring of the test circuit including hookups.

A-2. Initialize the oscilloscope for current-voltage (I vs V) measurements, as follows:

- 1) Set CH1 mode = GND. And then align (horizontal) trace to axis.
- 2) Set CH2 mode = GND. Then align (horizontal) trace to axis.
- 3) Reset both CH1 and CH2 to mode = DC
- 4) Set display to XY mode.

When the amplitude of the input signal is at zero or the CH set at GND the output should appear to be a small dot in the center of the O-scope screen. Readjust the XY dot by means of the channel offset adjustment setting until it is moved to the upper left corner of the O-scope screen but offset by 1cm from left and top edges. This setting should allow maximum screen space for first-quadrant measurement (as inverted) of the transistor characteristics.

A-3. Adjust the signal generator to approx 8V pk-pk at $f_S = 1\text{kHz}$ and vary V_{BB} to see the onset of transistor forward characteristics. You should find that the trace (which will look like a bent wire) resembles a single trace out of the 'family of traces' represented by figure 5.2b, except upside down (as shown by figure 5A-3). Also expect some hysteresis with the oscscope trace. Reduce f_S until the hysteresis is suppressed, which will probably leave your sweep at approximately 50Hz.



Figure 5A-3. Expected output trace for part A-3.

A-4. Set V_{BB} to 1.0 VDC. Measure V_C at the "knee" of the curve and at least three values above the "knee" (i.e. along the approx horizontal part of the trace). Since the slope is almost flat you may have to increase amplification and shift the origin to realize a measure of the slope in this (active-mode) regime. Be sure and include an error estimate in your data table.

A-5. Repeat measurements for at least 5 values of V_{BB} ranging from 1.0V to 6.0VDC. For each setting of V_{BB} also measure V_B using the DMM. You can reset amplification factors and adjust fiducial origin of the trace as you see fit. It is good form to indicate the different scope settings when you are using it and changing amplification scaling for making your measurements

A-6. Replace the test frame resistance set with $R_{BB} = 1\text{M}\Omega$, $R_X = 10\text{k}\Omega$ and $R_Z = 1\text{k}\Omega$ and repeat the measurements of parts A-4 and A-5. Expect more hysteresis and noisier measurement levels. Be wary of limits imposed by the test frame, since they can distort and flatten your measurements. Make accommodations as necessary to accomplish a good set of measurements.

B-1. Replace the 2n3904 transistor with the 2n3906 transistor and reverse polarity of V_{BB} and of diode D1. Repeat the setup process and measurement sequence of part A. A typical scope trace for the *pn*p output characteristics as viewed by the test frame is shown by figure 5B-1.

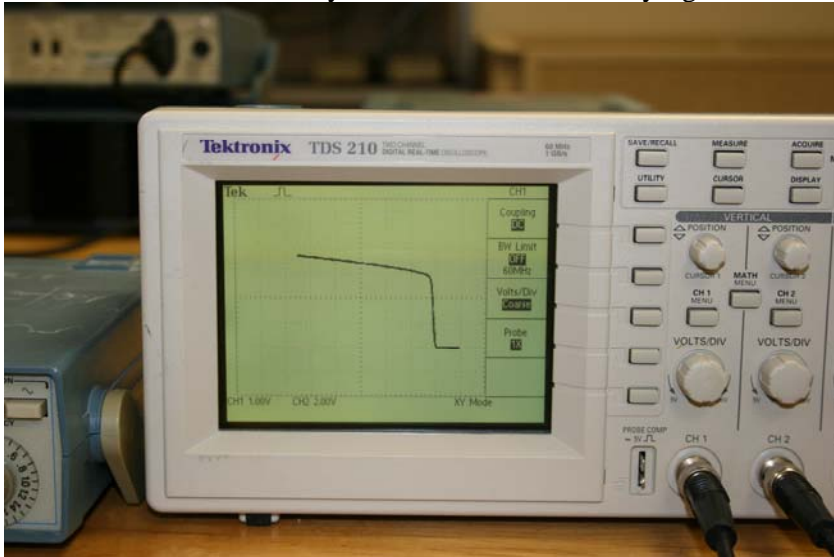


Figure 5B-1. Expected output trace for part B-1. The *pn*p transistor has a much more pronounced slope in the active regime (i.e. smaller Early voltage V_A) than that of the *npn* transistor. Note that the fiducial origin of the trace has been moved to the lower right corner to accommodate the polarity switch of the transistor and inverted transfer curve.

ANALYSIS: Some of the voltage measurements will need to be translated into current values and can be accomplished by the following relationships, most of which are self-evident:

$$I_B = (V_{BB} - V_B) / R_{BB}$$

$$I_E = V_Y / R_E$$

$$I_C = I_E - I_B$$

$$V_{CE} = V_C \text{ (since } V_E \text{ is at virtual ground, courtesy of the opamp)}$$

A. For each of the settings of the resistance bias frame use your spreadsheet to create an (overlaid) plot family of I_C vs V_{CE} (use the X-Y plot function) for which each (input) value I_B defines a trace. Don't forget to include the default value $I_C = 0$ at $V_{CE} = 0$ (which is not part of your measurement set but is understood).

B. Determine the forward current gain $\beta_F = I_C / I_B$, where the value of I_C is the value of current just above the transition 'knee'. The forward current gain β_F should not be expected to be a constant, regardless of what you may have been told in class. Create an XY plot of β_F vs $\log(I_C)$ as part of your exposition and report. You should find out that β_F is affected by current level.

C. Determine measured slope $\Delta I_C / \Delta V_{CE}$ above the "knee" for each member of the family of traces. Slope $\Delta I_C / \Delta V_{CE}$ is called the collector output conductance, also identified as g_O . Plot g_O as a function of $1/I_B$. For each value of g_O identify the level of output current I_C just above the "knee" as part of your extracted data.

D. Using the information of part C determine the Early voltage V_A as defined by the relationship $g_O = I_C/V_A$. Expect V_A to be approximately a constant, with some mild variation. Determine average and approximate variance (error) of this value. Make an X-Y plot of V_A vs I_B using the Excel plot menu.

E. Confirm results of parts A-D by means of spice simulation. Unlike the bench tests pSPICE can acquire transistor characteristics by means of an ideal (IDC) current source I_B at the input (in place of R_{BB} and V_{BB}) and a DC-sweep of V_C . The trace of I_C vs V_{CE} with step of I_B is accomplished by means the ‘**Nested sweep**’ option under **Analysis>DC Sweep**. Step the source I_B through 4-5 steps at the appropriate levels to create a plot family for your lab report. The upper limit of the ‘DC sweep’ of V_{CE} should be at least 5V. The pSPICE I_C vs V_{CE} plot family should be set in side-side comparison to that of part A

F. Now recreate the Excel plots of parts C and D using pSPICE. Create a fine-grained version of I_C vs V_{CE} but with I_B declared as a parameter by use of the designation $\{I_B\}$ and a PARAMETER table. Step I_B as a *Parametric* variable (**Analysis > Parametric**). The same plot family as for part B will result, except with more traces. Do not make a plot of I_C vs V_{CE} in this case since you will have an overload of data, and all you really require is the slope in the active regime.

G. As a consequence of use of I_B as a parameter in part F the ‘Performance Analysis’ option on the PROBE postprocessor can be invoked. This option will allow you to make use of the following ‘goal function’. You can copy the text string (below) and paste it into the trace command line

YatX(IC(Q1)/D(IC(Q1))/D(V_VCE),2.0)

and it will directly realize a pSPICE plot of $V_A = I_C / (dI_C / dV_{CE})$ as evaluated at $V_{CE} = 2.0V$.

Compare simulation and experimental results by displaying the X-Y plot of part D and the pSPICE plot of part G side-by-side. They may not match all that well but should be of the same order of magnitude.

H. Using the set of traces generated by pSPICE under part F create a plot of the forward current gain β_F vs I_B . This plot can be realized by means of the same techniques as that of part F (i.e. step I_B using the **Analysis > Parametric** option) and the goal function

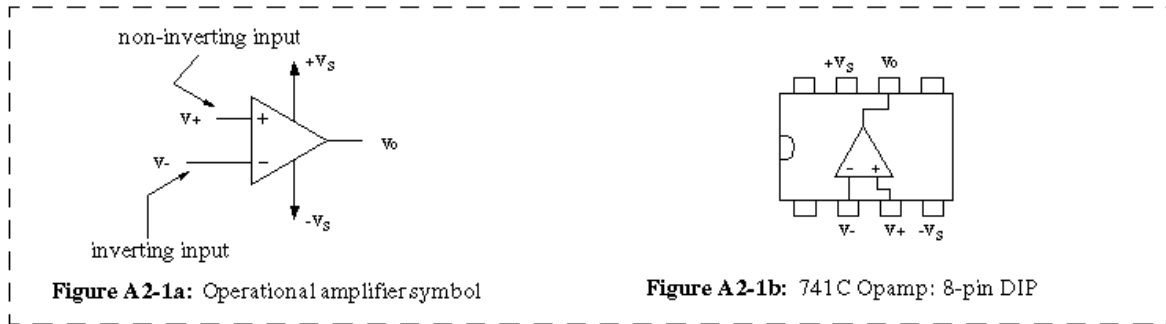
YatX(,)

where the second argument should also be chosen to be $V_{CE} = 2.0$ (which is the same value as used in the goal function of part G).

Compare simulation and experiment by displaying the plots of part B (= measured β_F) and part H (= simulation β_F) side-by-side.

Look up the pSPICE parametric values of V_A and β_F by the model statement (**Edit > Model > Edit Instance Model (text)**) for parts Q2n3904 and Q2n3906 and compare these to your extracted results. In the model parameter list V_A and V_{af} are synonymous, and your result should not be radically different. On the other hand your value of β_F will not likely agree with the model parameter Bf since β_F has an equation of its own and varies with I_C .

APPENDIX A-1: Pinout for 741C opamp



APPENDIX A-2: Diode and capacitance parts.

