ECE3424 Electronic Circuits Laboratory

Experiment #6 Optimization of single-transistor BJT amplifiers vers 2.4

OBJECTIVE: Measure transfer characteristics of a single-transistor BJT amplifiers and qualify circuit distortion in terms of the effect of the bias network of resistances.

Background: An amplifier is effectively represented by the two-port model of figure 6.1. The output signal is labeled as v_L because it is applied across the load R_L. The characteristics of the transfer circuit include an input resistance R_{in} and an output resistance R_{out} as well as the transfer gain A_V.

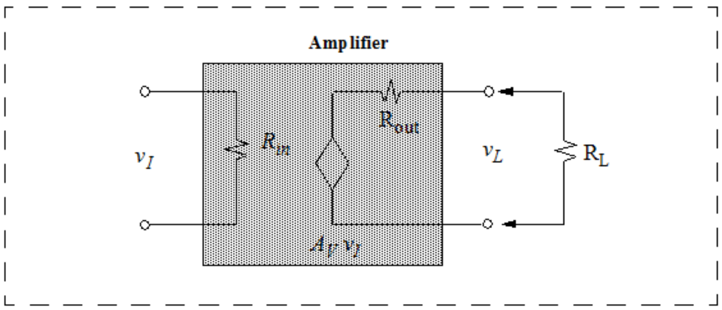

Figure 6.1 Amplifier characteristics

These signals and amplifier transfer characteristics are all based on small increments of voltage at the input and output, for which $\Delta V_I = v_I$, $\Delta V_L = v_L$. Consequently the input and output resistances are not just equivalent resistances but include components that are slopes. For example $R_{in} = v_L/v_I = dV_I/dI_I$. So measurement cannot be done by a DMM.

PROCEDURE:

A-1: The amplifier topology that we will consider is by figure 6A-1. This topology is defined as the *common-emitter* (CE) configuration, and is a general-purpose amplifier topology.

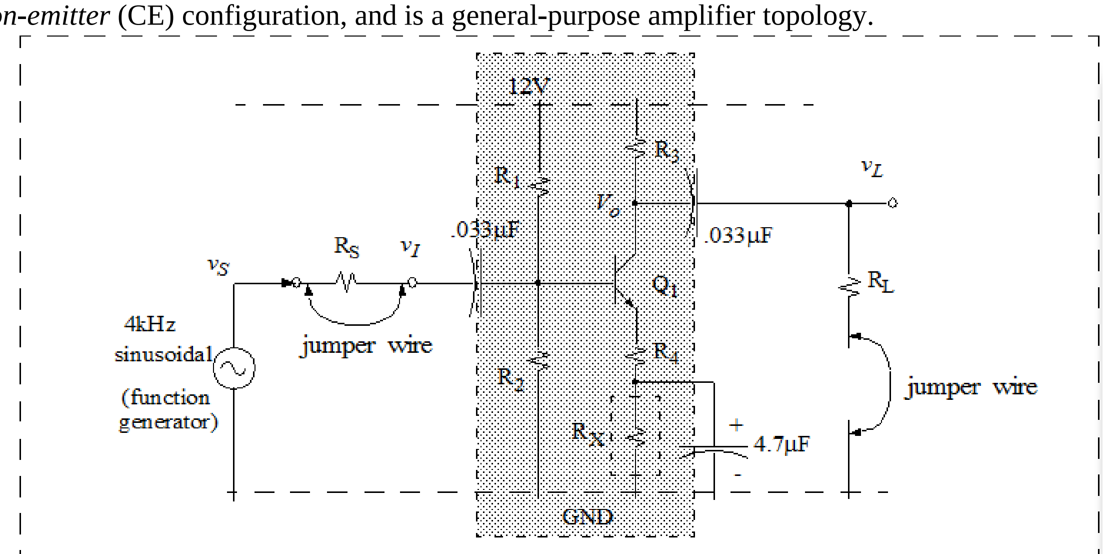

Figure 6A-1. Common-emitter (i.e. general purpose) configuration for test of amplifier characteristics

The construct is effectively a frame of components (resistances and transistor) strung between two voltage rails. In this case the upper rail is a 12V power supply and the lower rail is at ground. Resistance values are as follows: R_1 = 220kΩ, R_2 = 100kΩ, R_3 = 22kΩ, R_4 = 333Ω || 1.0kΩ, R_L = 22kΩ and R_S = 47kΩ. R_X is the resistance box, set initially to 10kΩ.

Q_1 is a 2n3904 general-purpose switching transistor For reasons of frequency response the CE topology requires a relatively large capacitance at the emitter which requires that we make use of an *electrolytic* capacitance (i.e. contain an electrolyte). Be aware that it must be oriented so that its polarity is accommodated. Otherwise the capacitance will short out and explode.

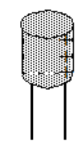

Figure 6A-2: Electrolytic capacitance

A-2: Set up the circuit of figure 6A-1 on the prototyping motherboard with V_+ = 0 VDC (temporarily) and the amplitude of the signal generator reduced to zero. Transistor Q_1 is the 2n3904. Figures 6A-4a and 6A-4b should help with placement and wiring considerations. Transistor leads for the BJT are identified by figure 6A-3.

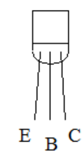

Figure 6A-3: Transistor leads

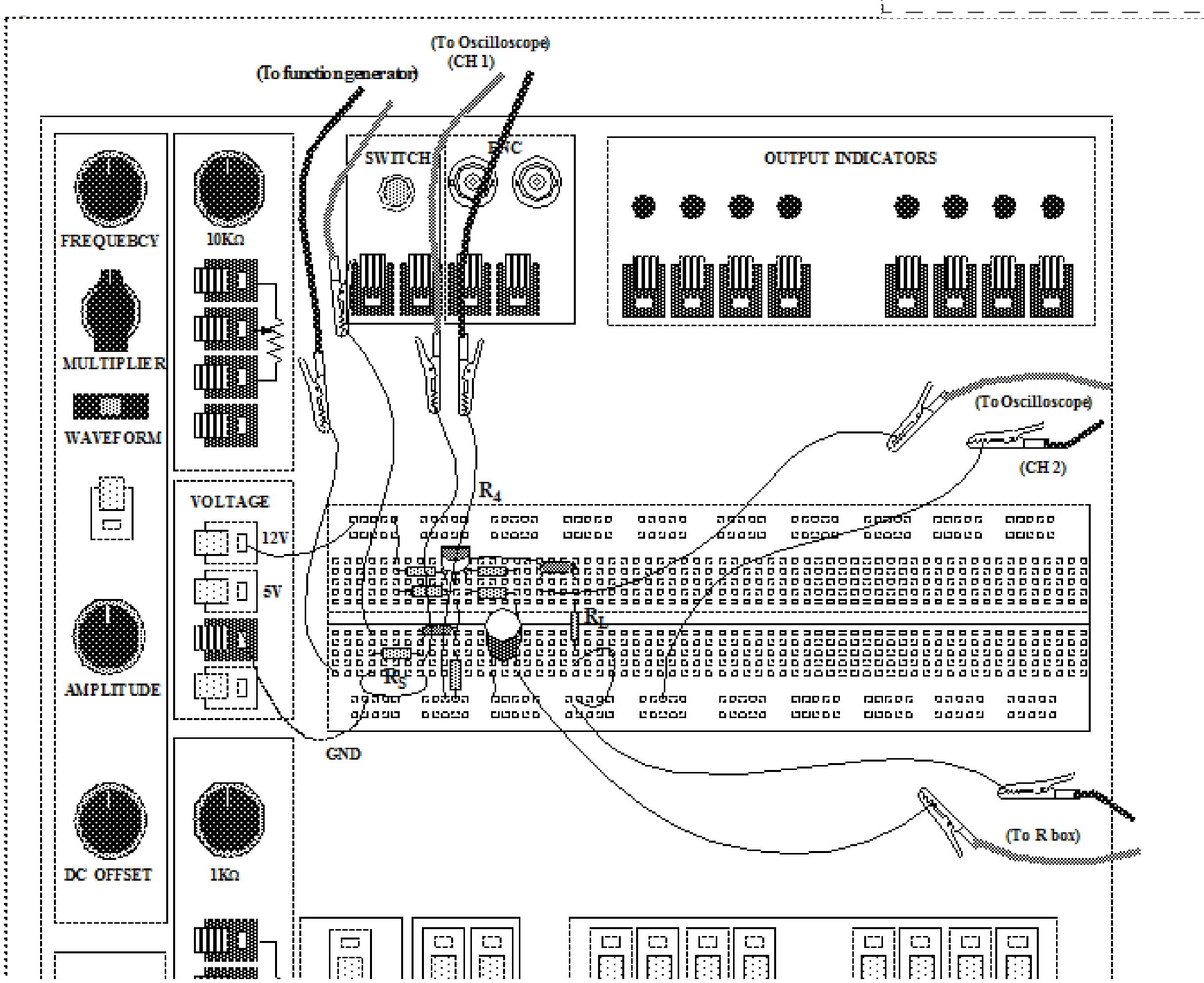

Figure 6A-4a Suggestions for placement and wiring.

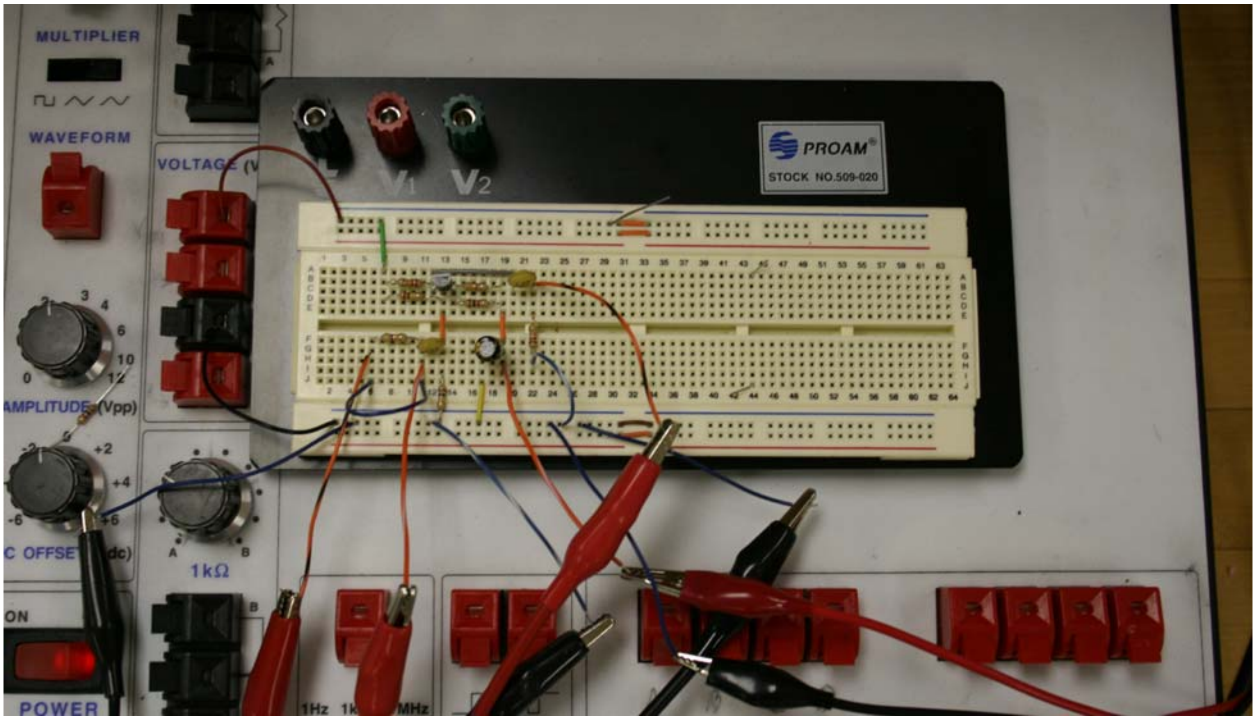

Figure 6A-4b Suggestions on placement and wiring. Photo.

As represented by figures 6A-4a and 6A-4b, if you lay out the circuit on the protoboard with roughly the same topology as the circuit diagram itself there is less aptitude for wiring error.

A-3. The reason that R_4 is chosen as the parallel combination 330Ω||1.0kΩ, is because it is desired that R_4 be switched between values of 0.25kΩ and 1.0kΩ, which is readily accomplished by pulling the 330Ω free. On the other hand resistance R_3 switched between 10kΩ and 22kΩ by exchange. Load resistance R_L and source resistance R_S are switched in and out by the jumper wires, which should also be fairly visible on the placement and wiring figures.

Resistance R_X is switched between values of 10kΩ and 50kΩ by toggling the *Rbox* settings. This resistance essentially controls the current through the transistor. The detailing for which a current level is defined from R_X is left to the spreadsheet. Set it initially to R_X = 10kΩ.

A-4. Once everything is wired turn on the 12V power supply and snake check the circuit by use of the DMM probes to check the voltages at the base (V_B), emitter (V_E) and collector (V_C). Expect V_B and V_E to be approximately 3.6V and 2.9V respectively. Assurance that the transistor is conducting is confirmed when its node values fall between the power rails. If the transistor is not ON its node values will either be 12V or 0V.

A-5. Insert the jumper wires as indicated at the input and outputs. Apply a 10kHz signal with peak-peak amplitude 400mV to the input. Output peak-peak amplitude should be considerably larger than that of the input amplitude (on the order of 1.5V) but so badly distorted that it would be meaningless to make any transfer gain measurements. A typical output, with distortion, is shown by figure 6-5. If input amplitude is increased you should see the output signal distorted at both lower and upper extrema.

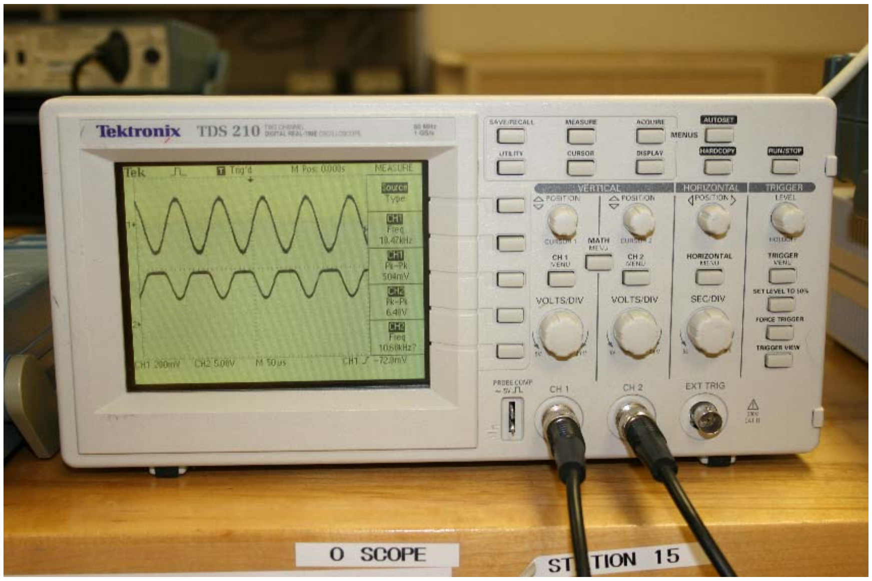

Figure 6-5 Distortion limiting of the output signal.

A-6. Execute the test series shown by table A-6.1 indicating whether the output is doubly distorted or distorted at one extreme. Apply the CH2 tap to V_C rather than V_L since the output at V_C will tell you more about the origins of the distortion. Set the CH2 scope trace to 'DC coupling', increase the input until output distortion results at both upper and lower extrema and determine values for these distortion limits from the DC values of the scope traces. You may have to flip back and forth between 'DC coupling' and 'GND' settings of CH2 to make a relative measure between GND and the distortion (compliance) limits.

Table A-6.1: Test matrix and spreadsheet data table for f_S = 10kHz, V_S = 400mV pk-pk

R3	**R4**	**RX**	**Distortion (upper, lower)**	**Distortion limit value(s)**
22kΩ	250Ω	10kΩ		
22kΩ	250Ω	50kΩ		
22kΩ	1.0kΩ	10kΩ		
22kΩ	1.0kΩ	50kΩ		
10kΩ	250Ω	10kΩ		
10kΩ	250Ω	50kΩ		
10kΩ	1.0kΩ	10kΩ		
10kΩ	1.0kΩ	50kΩ		

B-1. Reduce input signal level V_S (as much as possible subject to noise) until distortion is no longer evident and take measurements of A_V and R_{in} for all settings of table A-6.1. Figure B-1.1 should be a sufficient guide for these tests. The assessment of R_{in} is accomplished by measurement of v_L via the 'measure' button on your O-scope) with the shorting wire at the input alternately connected and disconnected. Some settings may preclude reasonable measurements because of distortion. Let the distortion tests of part A be your guide. It will probably be to your advantage to keep the output loaded by the resistance R_L for measurement of R_{in}, but you will also have to measure the output under no-load conditions (i.e. R_L disconnected) in order to determine transfer gain A_V.

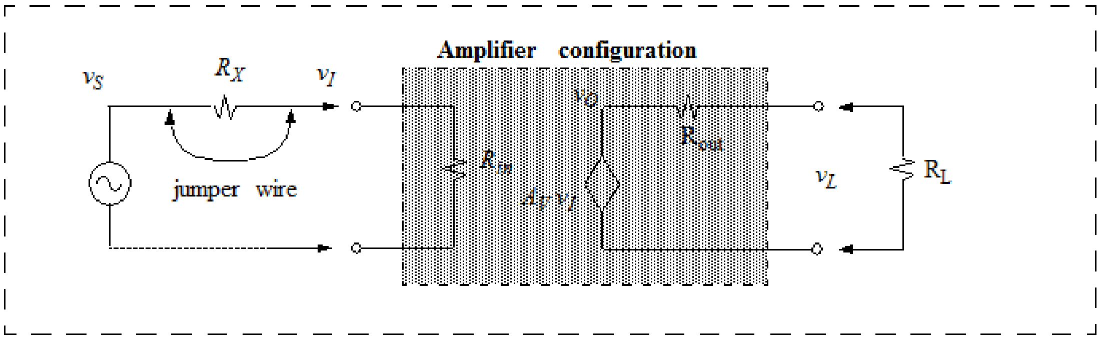

Figure B-1.1. Measurement of input resistance and transfer gain.

If you take the output off v_L, then R_{in} is measured by the ratio (use spreadsheet to extract R_{in}).

$$\frac{v_L(OFF)}{v_L(ON)} = \frac{R_{in}}{R_{in} + R_X} \qquad (6B\text{-}1)$$

where $v_L(OFF)$ is with input jumper disconnected, and $v_L(ON)$ is with input jumper connected.

B-2. In like manner measure the output resistance by means of the jumper wire at the output.

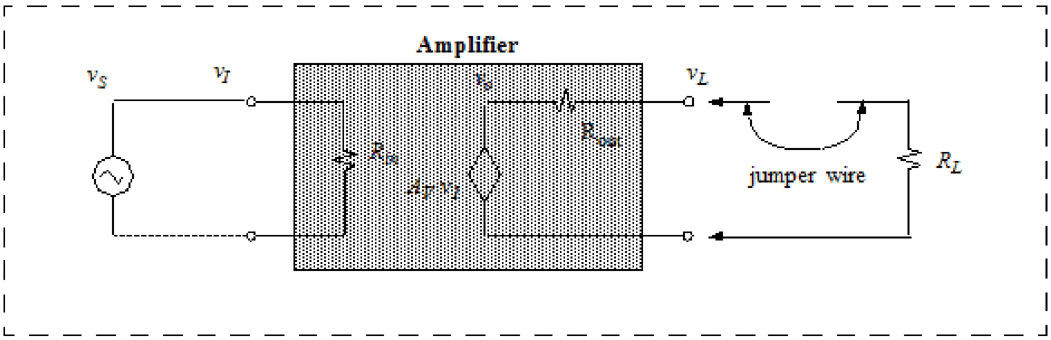

Figure B-2.1 Measurement of output resistance.

In like manner, with measurement at output node v_O then R_{out} is measured by the ratio (use spreadsheet to determine R_{out}).

$$\frac{v_O(ON)}{v_O(OFF)} = \frac{R_L}{R_{out} + R_L} \qquad (6B\text{-}2a)$$

where $v_L(ON)$ is with jumper to load connected, and $v_L(OFF)$ is with jumper to load disconnected.

(variant 2): If you have inserted a resistance R_X between the output of the amplifier and the load R_L, and deployed the jumper wire across R_X then you should expect that the ratio should be a little more complicated but still viable, namely

$$\frac{v_O(ON)}{v_O(OFF)} = \frac{R_L}{R_{out} + R_L} \times \frac{R_{out} + (R_L + R_X)}{(R_L + R_X)} \qquad (6B\text{-}2b)$$

and you will need more algebra to solve for R_{out} (recommend that you divide all R's by R_L). The spreadsheet should then do the calculation.

(variant 3): Another option is that you could have taken the output off v_L, and then used a jumper to take out R_X in like manner to variant 2 in which case the ratio is then

$$\frac{v_O(ON)}{v_O(OFF)} = \frac{R_L}{R_{out} + R_L} \times \frac{R_{out} + R_X}{R_L + R_X} \qquad \text{(6B-2c)}$$

and you will need some other algebraic usage to solve for R_{out} (recommend that you divide all R's by R_L). (The spreadsheet should then do the calculation.)

Whatever variant is/(was) employed the result should be the same.

ANALYSIS and REPORT:

1. The following relationships are the small-signal analytical relationships for the transfer characteristics associated with the CE (general purpose) topology:

$$R_{in} = R_1 \| R_2 \| R_{iB} \qquad \text{where} \qquad R_{iB} \cong \beta_F \times \left(\frac{1}{g_m} + R_4 \right)$$

$$R_{out} = R_3 \| r_{out} \qquad \text{where} \qquad r_{out} = r_o \left(\frac{\beta_F \left(1/g_m + R_4 \right)}{\left(\beta_F / g_m \right) + R_4} \right)$$

$$A_V = \frac{v_L}{v_I} \cong -\frac{R_3 \| R_L}{1/g_m + R_4} \qquad g_m = 40 \times I$$

and $I \cong \left(V_{BB} - 0.7 \right) / \left(R_4 + R_X \right)$ for which $V_{BB} = \dfrac{R_2}{R_1 + R_2} \times 12.0V$

As an approximation we may accept defaults r_o = 100kΩ and β_F = 100

2. Complete your data table with columns that compare A_V, R_{in}, and R_{out} as evaluated by the analytical relationships with the values as measured. Comment on comparisons and accuracy of measurement.

3. Use the results of your measurements to determine the best-fit value for forward current gain β_F of the 2n3904 transistor.

4. What are your conclusions about the effect of the resistance bias network on the compliance limits of the transfer characteristics?

5. Execute a pSPICE simulation of figure 6A-1 by means of a <u>transient analysis</u> for the case in which R_L = infinity, R_3 = 22kΩ, R_4 = 250Ω and with R_X stepped from 10kΩ to 50kΩ in 4 steps. Compare your results with the compliance limits reflected by pSPICE to those that you determined.

In addition and concurrently to the transient analysis displays of $V(V_L)$, invoke a Fourier analysis (**Analysis>Transient>Enable Fourier**) for output = $V(V_L)$ and center frequency = 10kHz with 10 harmonics. The Fourier output results will be listed as a text file under **Analysis>Examine Output**, probably toward the bottom of the file. List the THD (total harmonic distortion) for each case as part of your data analysis.

6. Design a CE general purpose amplifier (i.e. identify a complete set of bias frame resistance values R_1, R_2, R_3, R_4, and R_X) which makes use of a 12V supply as used by the experiment and yields a 5.0V pk-pk output at 10kHz to an R_L = 120kΩ load with no more than 5% THD, with transfer gain A_V = 25V/V and R_{in} = 50kΩ or larger. (Hint: Use pSPICE as a test bed and step R_X). You will need to elect different values for all resistances, including R_1 and R_2. Include a pSPICE simulation as confirmation, with schematic, and show the Fourier table (which will display the output amplitude and the THD of your design).