

ECE3424 Electronic Circuits Laboratory

Experiment #8 Conduction characteristics of the junction Field-Effect Transistor Vers. 2.4

OBJECTIVE: Measure conduction characteristics of an n-channel Junction Field-Effect Transistor (nJFET) and extract first-order model parameters.

Comments: Most discrete transistors are *pn* junction devices. Of these there are two basic type transistors: (1) BJTs and (2) JFETs. BJT's have two junctions. Junction FETs have only one and therefore are also called unijunction transistors. Both BJTs and JFETs are moderate-to-high current devices. And both are tough and can handle reasonably severe electrical challenges and students

For the JFET conduction takes place by means of a buried conducting channel that is controlled by the reverse-bias field of the junction. In that respect it is not unlike the operation of the more familiar MOSFET, for which the conducting channel is at the surface and controlled by a capacitance field applied to the surface to induce a surface conduction channel.

In this experiment we will examine and evaluate the characteristics of the JFET. The symbol for the JFET and its typical package are represented by figure 8-1b.

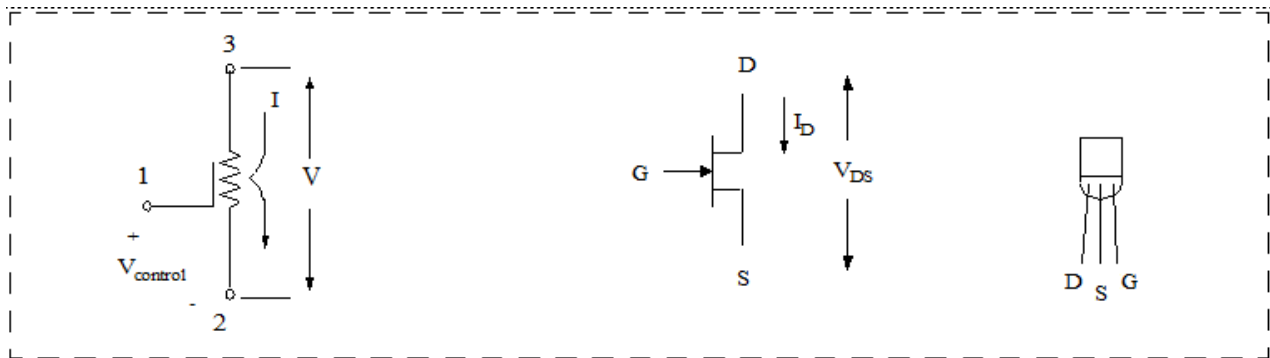


Figure 8-1a Generic transistor

Figure 8-1b. junction Field-effect transistor

For the FET, output characteristics are usually specified in terms of I_D vs V_{DS} , as indicated by figure 8-2b. Unlike its cousin, the bipolar junction transistor (BJT), the jFET is bilaterally symmetric, a property we will confirm with the measurement sequence.

The control terminal is called the gate, and it is the gate-source voltage V_{GS} that defines the 'ON' characteristics of the FET. V_{GS} must be greater than V_P , where V_P is called the 'pinch-off' voltage, and represents a threshold below which the conducting channel is 'pinched off'. Magnitude of the output current I_D is proportional to $(V_{GS} - V_P)^2$, and usually is on the order of mA. The output characteristics of the FET are typically of the form as represented by figure 8-2b. The low-drain-field transfer characteristics I_D vs V_{GS} are represented by figure 8-2c.

For the nJFET V_{GS} must be negative. In fact if $V_{GS} > 0$ the gate junction becomes forward-biased and the channel current is no longer under control of the gate field and the transistor is no longer a control device.

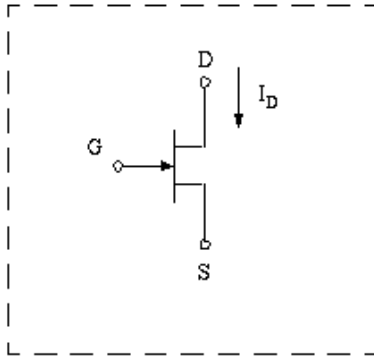


Figure 8.2a nJFET

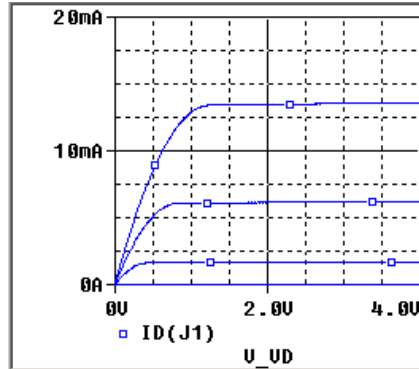


Figure 8.2b Output characteristics

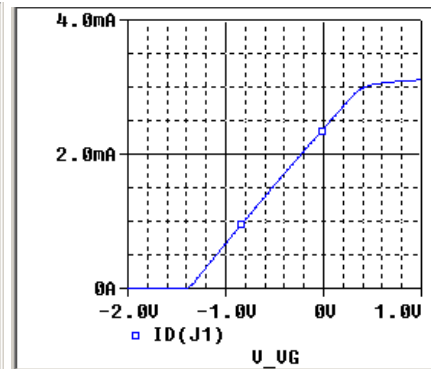


Figure 8.2c Transfer characteristics

The JFET is a field-effect device and is adequately described by the equations

$$I_D = \beta \left[(V_{GS} - V_P)V_{DS} - \frac{1}{2}V_{DS}^2 \right] \quad \text{for } V_{DS} < (V_{GS} - V_P) \quad (8-1a)$$

$$I_D = \frac{1}{2} \beta (V_{GS} - V_P)^2 \quad \text{for } V_{DS} > (V_{GS} - V_P) \quad (8-1b)$$

where $\beta \equiv$ conduction coefficient and $V_P \equiv$ pinch-off voltage. These equations are the same as those of the MOSFET, with exception that the MOSFET uses a threshold voltage V_{TH} instead of pinch-off voltage V_P . The conduction coefficient β may be switched with an equivalent coefficient, $2K$, for which K may be also defined as the conduction coefficient, depending on the reference. The conduction coefficient also may be defined in terms of the maximum allowed current through the JFET, I_{DSS} , for which

$$I_{DSS} = \beta V_P^2 / 2 \quad (8-2)$$

There is always a slight slope for increase of V_{DS} , as represented by figure 8.2b

$$\frac{dI_D}{dV_{DS}} = g_o = \frac{I_D}{V_A} \quad (8-3)$$

In the measurement process we will also be interested in finding a value for parameter V_A . V_A is called the Early voltage (after James Early, and early researcher in transistor devices).

PROCEDURE:

Preliminary: The junction FET has a single junction that controls the buried channel. The 2n5457 is an nJFET. It therefore has a p -type gate that controls an n -type channel. Using your DMM set to the resistance measurement mode determine which of the device terminals is the gate (i.e. test for forward and reverse bias of the junction). Your findings should be consistent with figure 8-1b of the 'Comments' section.

The test circuit topology for assessment of the conduction characteristics of an nJFET (2n5457) is shown by figure 8A-1. A large amplitude triangular-wave signal is applied across the transistor by the signal generator. Current is measured by the voltage across R_X , which also serves as a current-limiting resistance for the extreme case in which the transistor is fully conductive. Diode D1 is oriented so that only the positive swing of the AC signal will be applied across the circuit, keeping measurements in the first quadrant. V_B is the external variable power supply and is applied to a 5:1 voltage divider that both serves to bias the JFET into a conduction state and limits the gate current, should the transistor junction be driven into forward bias. The unity-gain opamp inverter will recast the output characteristics so that they will be of the 'normal' form like those represented by figure 8-2b of the 'Comments' section.

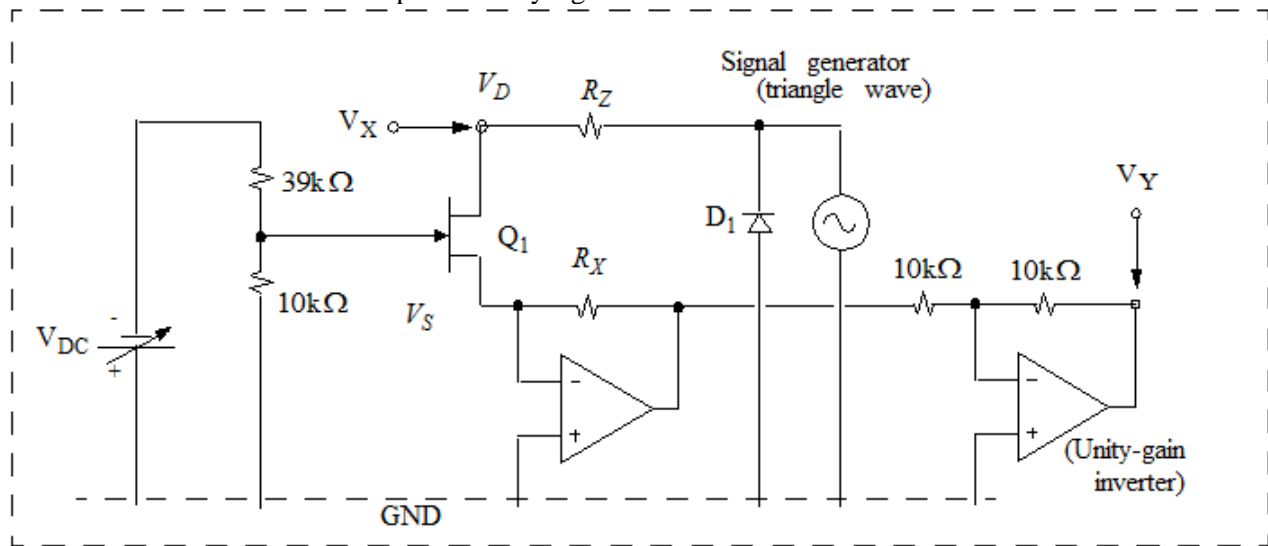


Figure 8A-1. Test frame for measurement of n-channel junction Field-effect transistor (nJFET) drain characteristics

A-1. Set up the circuit of figure 8A-1 on the protoboard with $V_{DC} = 0$ VDC and the amplitude of the signal generator reduced to zero. CH1 should be connected to V_D and CH2 to the output of the second opamp (unity-gain inverter) as shown. Resistance $R_X = 1.0k\Omega$ and $R_Z = 100\Omega$. Transistor J1 is 2n5457 n-channel JFET. The 2n5457 is listed as having $I_{DSS} = 5\text{mA}$.

Placement and wiring suggestions are shown by figures 8A-2a and 8A-2b

A-2. Initialize the oscilloscope for current-voltage (I vs V) measurements, as follows:

- 1) Set CH1: mode = GND. And then align (horizontal) trace to axis.
- 2) Set CH2: mode = GND. Then align (horizontal) trace to axis.
- 3) Reset both CH1 and CH2 to mode = DC
- 4) Set display to XY mode.

With the amplitude of the signal generator at zero, the output as initialized should be a small dot in the center of the O-scope screen. If not, adjust the offsets on each channel so that the dot is at center.

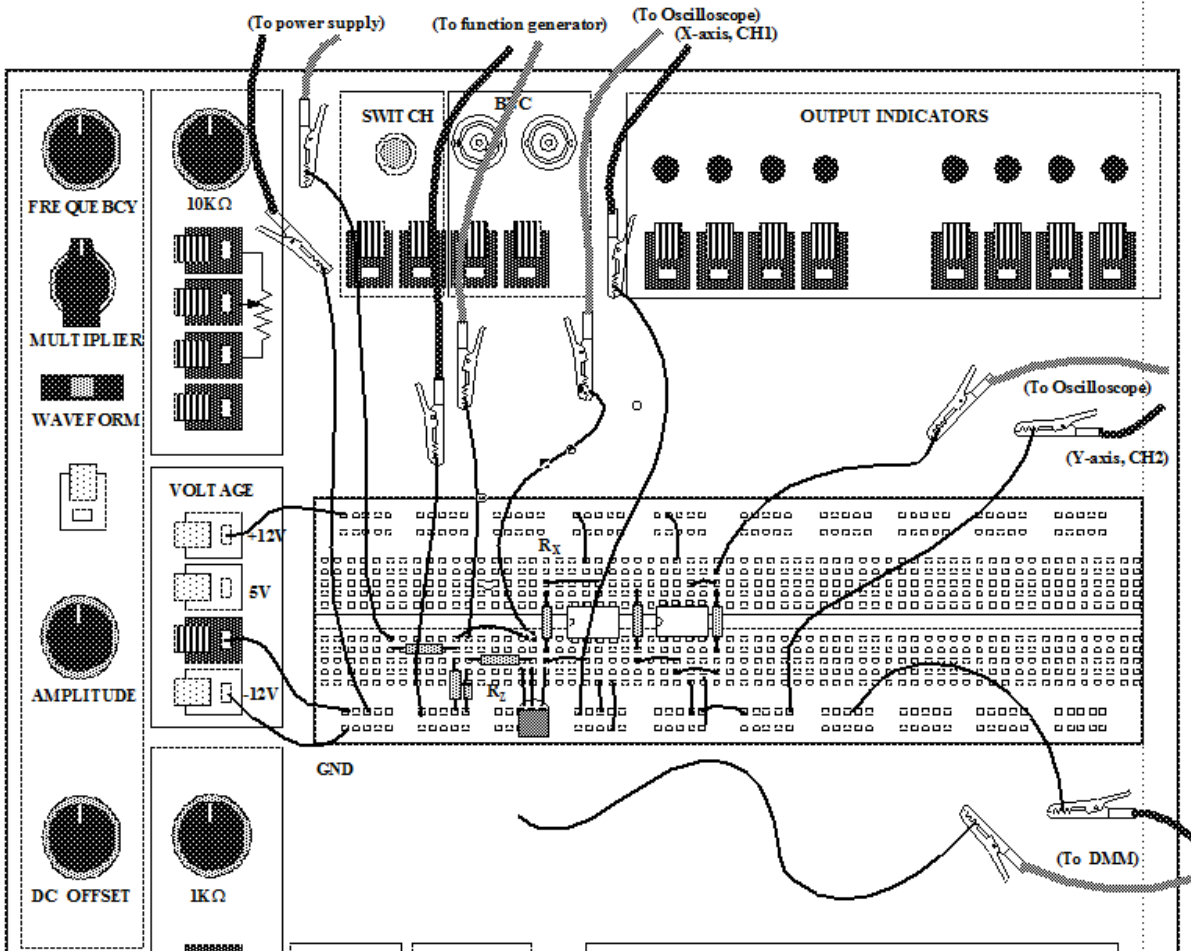


Figure 8A-2a Suggested placement and wiring for the nJFET test circuit.

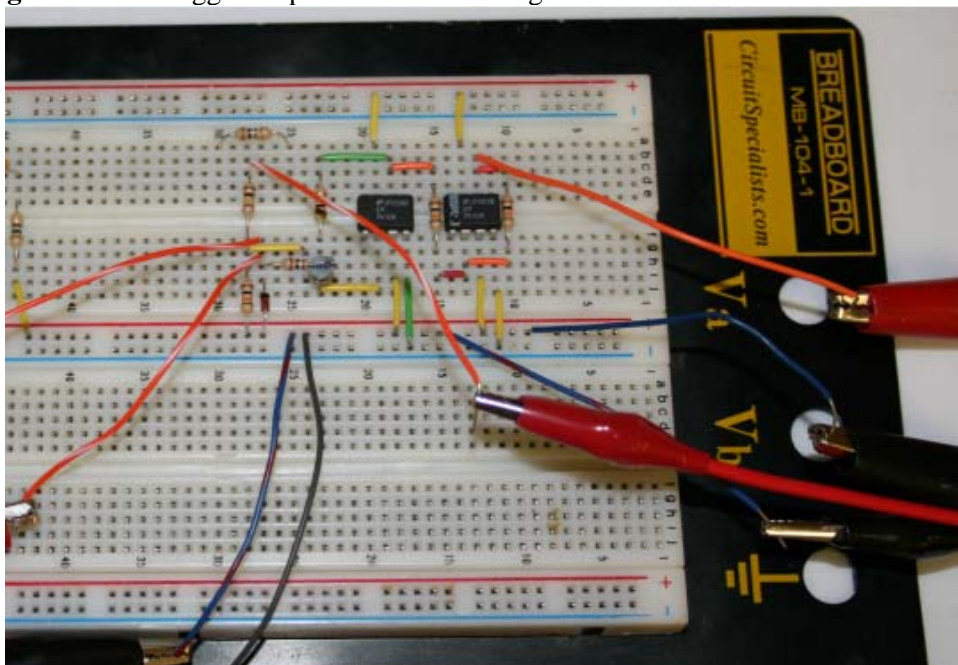


Figure 8A-2b Photo of placement and wiring of figure 8A-1 (nJFET test circuit.)

B-1 With $V_{DC} = 0$, adjust the signal generator to amplitude 7.0V (14V pk-pk) at 100Hz to see onset of transistor forward characteristics. You should see a trace that looks something like that of figure 8B-1. If your circuit is connected properly, the reverse swing of the signal generator should be limited by diode D1 to approximately 0.5 cm of scale for the swing of V_X in the 4th quadrant.

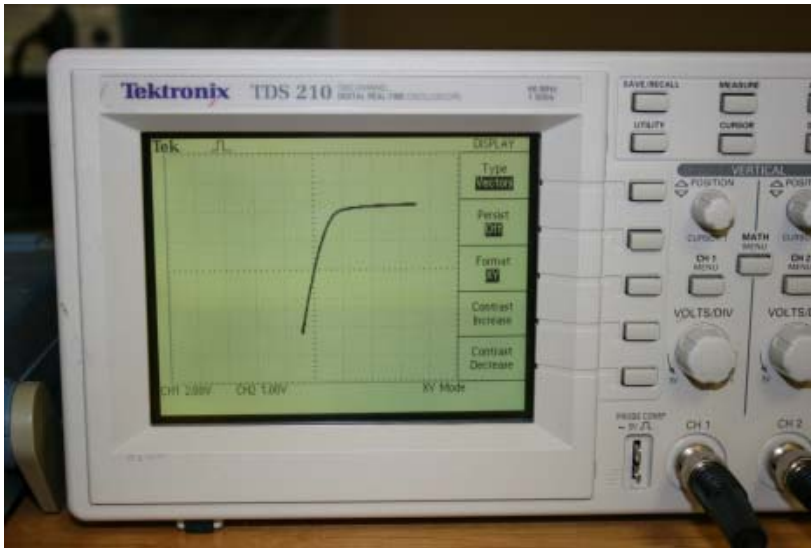


Figure 8B-1. Scope trace output for part B-1

B-2. Reduce the signal generator amplitude and V_{DC} to zero and relocate the trace center (which should now show up as a dot in XY mode) to the lower left corner, but offset by 1cm from left and lower boundaries. This setting should allow you to have the maximum screen space for first-quadrant measurement of the transistor characteristics through adjustment of the range settings for CH1 and CH2.

B-3. Apply full signal generator amplitude to the circuit. From the O-scope trace measure the value of V_Y at the onset of saturation (just above the knee of the curve). Keep in mind that V_Y is equates to drain current I_D via resistance R_X . So you are effectively evaluating I_D vs V_X , where $V_{DS} = V_X$.

The measurement for the JFET is not unlike that undertaken for its BJT cousin (earlier experiment) except that the conduction level of the transistor is defined by V_{GS} .

B-4. Determine the slope $\Delta V_Y / \Delta V_X$ for the curve trace above the knee. Make use of the gain and offset controls to obtain a reasonable measurement. You do not have the advantage of a cursor in the X-Y mode, so expect some slop in your measurements. Make an error estimate.

*You actually can flip back and forth between X-Y and X-t mode to make use of the cursor for slope measurements if you so desire, but you will need to correlate X-t waveforms and the X-Y characteristics.

B-5. Readjust $V_{DC} = -2.0$ V (equivalent to applying a V_{GS} of -0.4V to the gate as consequence of the voltage divider) and repeat parts B-2 thru B-4) for V_Y and slope $\Delta V_Y / \Delta V_X$.

B-6. Repeat the measurement process of part B-5 for V_{DC} stepped in increments of $\Delta V_{DC} = -1.0$ V until $V_{DC} = -8$ V or the level V_Y goes to zero. The pinch-off voltage V_P for this JFET should be approximately -1.5V, which corresponds to a V_{DC} of approx $(5 \times -1.5) = -7.5$ V.

C-1 Interchange the source and drain (flip the transistor and move gate connection). Repeat parts B2 thru B-6. The FET is bilaterally symmetric and this exchange should have little effect, but it must be confirmed since manufacturers sometimes add extra features that give preference to a particular orientation.

ANALYSIS:

A. From your measurements you should have achieved sufficient data to extract parameters for the 2n5457 JFET. Make plots as follows:

(a) $\sqrt{I_D}$ vs V_{GS} From this plot extract β and V_P using curve-fit techniques similar to those of previous experiments. Your data should approximately fit equation (8-1b), for which drain current I_D should relate to your V_G data via $I_D = V_G/R_X$.

(b) dI_D/dV_{DS} vs I_D From this plot and using curve-fit techniques extract the Early voltage.

B. Repeat for the measurements of the JFET for which D and S were interchanged.

C. Find the 2n5457 transistor in your pSPICE parts list and create plots of I_D vs V_{DS} and I_D vs V_{GS} . Choose values that enable you to make a one-one correspondence with your measurements and make comparisons. Comment on the differences and similarities. Compare your measurements of V_P , V_A , and β to those listed in the spice parameter listings (look under the menu **Edit>model>Edit instance model**).

D. Repeat part C (above) for the case in which D and S are interchanged,