

ECE3424 Electronic Circuits Laboratory

Experiment #9

Transfer characteristics for CMOS logic

Vers 2.12

OBJECTIVE: Evaluate transfer characteristics of CMOS logic gates in the transition regime.

Background: CMOS logic is a rail-to-rail logic technology. Logic levels V_{OH} (output high) and V_{OL} (output low) are a consequence of either the pull-up transistor set or the pull-down transistor set being off. The complementary set of transistors is ON and pulls the output against the power rail to which it is associated. Since one set of transistors is always off, CMOS draws no current when the logic state remains static.

But CMOS logic does draw current as it passes through transition. And the more transitions per second that occur, the more power is used. So the CMOS transition characteristics are critical. The transfer curve for a CMOS inverter is shown by figure 9-1b. The most primitive logic gate is the inverter (figure 9-1a) and it is used to benchmark the CMOS technology.

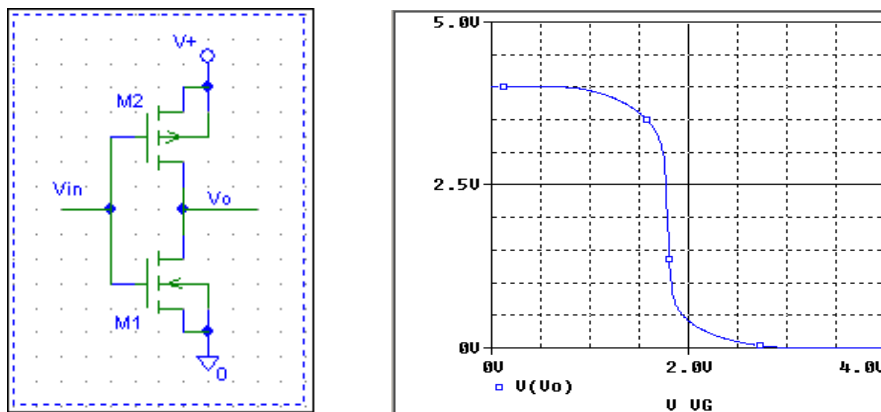


Figure 9-1a: CMOS inverter. **Figure 9-1b:** (Simulation) transfer curve for a CMOS inverter.

Logic states and margins are defined by the pull-down and pull-up devices, which are nMOS and pMOS transistors, respectively. As integrated circuits these transistors are not accessible to bench tests. But have no cause to fear. We can take the CMOS into places where no logic has gone before and smoke out most of the critical electrical information without resorting to violence.

All CMOS logic is an extension of the CMOS inverter. It is not uncommon to preset all but one input of a CMOS logic gate and then evaluate the remaining input as an inverter function, since it toggles the output in the same manner as that of figure 9-1b.

It is also possible to connect more than one input together and let the wired inputs toggle the output. Figure 9-2a shows such a choice for the NAND gate.

These options have the caveat of shifting the transition either high or low, as reflected by figure 9-2b. If the logic transition point is skewed logic faults can result. Thereby the charter of this laboratory exercise is to examine the CMOS logic family under transition and evaluate (1) transition skew factors and (2) dynamic power consumption represented by the transition current profile.

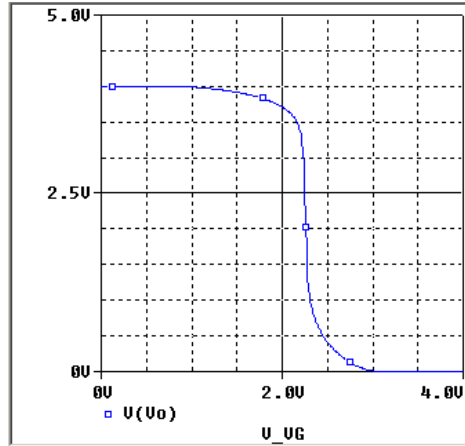
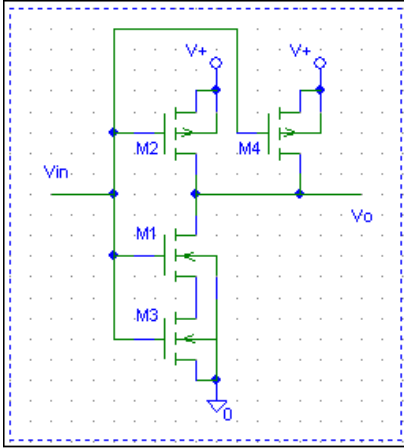


Figure 9-2a: CMOS NAND configured as inverter. $V_+ = 4.0\text{V}$.

Figure 9-2b: Transfer characteristics for figure 9-2a. The transition is shifted above midpoint $0.5V_+$.

The basic FET equations apply, for which

$$I_D = \beta \left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2 \right] \quad \text{for } V_{DS} < (V_{GS} - V_{TH}) \quad (9-1a)$$

$$I_D = \frac{1}{2} \beta (V_{GS} - V_{TH})^2 \quad \text{for } V_{DS} > (V_{GS} - V_{TH}) \quad (9-1b)$$

where $\beta \equiv$ conduction coefficient $= \mu_0 C_{OX} \times (W/L)$ and $V_{TH} \equiv$ threshold voltage. The conduction coefficient β may also be replaced by $2K$, for which K may also be defined as the conduction coefficient, depending on the reference.

CMOS (inverter) transition equations are as follows:

$$V_{IT} = \frac{V_+ + V_{TP} + \sqrt{K_R} V_{TN}}{1 + \sqrt{K_R}} \quad (9-2a)$$

$$\Delta V = V_+ + V_{TP} - V_{TN} \quad (9-2b)$$

$$I_{MAX} = \frac{K_N (\Delta V)^2}{(1 + \sqrt{K_R})^2} = \frac{K_P (\Delta V)^2}{(1 + 1/\sqrt{K_R})^2} \quad (9-2c)$$

$$\text{transition slope } \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{2(1 + \sqrt{K_R})^2}{\sqrt{K_R}} \times \frac{1}{(\Delta V [1/V_{A1} + 1/V_{A2}])} \quad (9-2d)$$

where $K_R = K_N/K_P =$ ratio of pull-down conduction coefficient to the pull-up conduction coefficient. These equations may be useful for curve-fitting measurements and extraction of buried information. They should also be of benefit for SPICE simulations.

PROCEDURE:

A-1. The test setup is shown by figure 9A-1. The configuration treats the CMOS inverter as if it were a weird transistor for which we desire to view and extract characteristics. The opamp pulls the lower supply rail of the CMOS logic gate to virtual ground. The opamp output will then yield an inverted profile of the transition current. Several bench test options are provided by V_{X1} , V_{X2} , and the jumper wire.

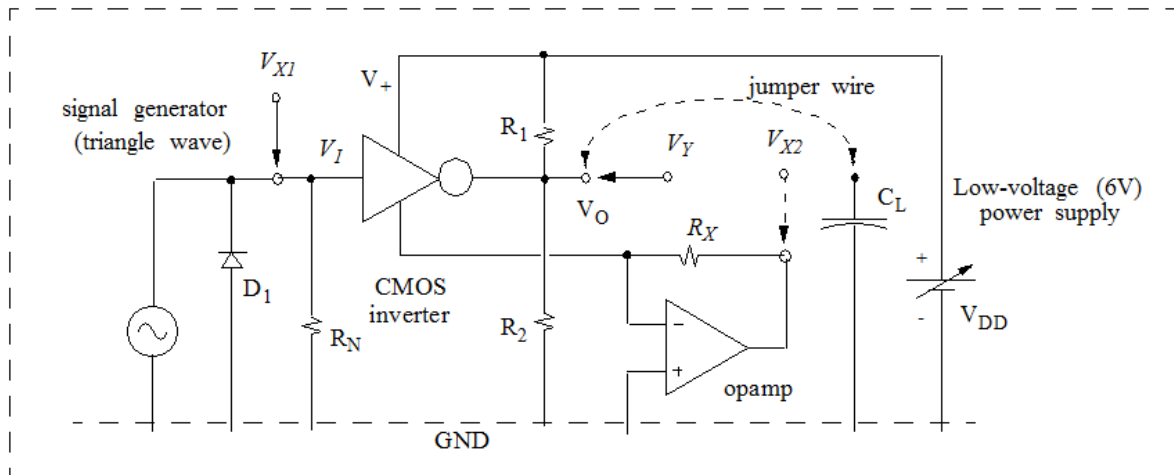


Figure 9A-1: Test set-up for evaluation of CMOS inverter transfer curve. In order to obtain V_O vs V_I we connect V_I to CH1 and V_O to CH2 of the O-scope (labeled as V_{X1} and V_Y , respectively, in the figure).

Resistance $R_N = 100\text{k}\Omega$ and is a default pull-down path when there is no input connection. Resistance $R_1 = R_2 = 10\text{M}\Omega$ are stabilization load paths and part of a later set of tests. R_X is a means of defining the level of current measure and is set to $10\text{k}\Omega$.

A-2. Construct the test topology of figure 9A-1 on your protoboard using the CD4069UBE CMOS hex Inverter (Do not use the CD74HC04E. It has noise problems). Pin-outs are in the appendix. Placement and wiring suggestions for figure A-1 are shown by figures 9A-2a and 9A2b. The opamp should be powered by the (+12, -12, GND) terminals of the MFJ box.

Set V_{DD} (6V variable supply) to 4.0V. The 6-V pushbutton switch on the power supply will connect it to power supply meter.

Use a jumper wire to manually toggle the input V_I alternately between GND and V_{DD} and confirm that the output toggles between high and low. This is a snake check test to ensure that the CMOS logic gate has not previously suffered an untimely fate at your hands or at the hands of others before you.

Initialize the oscilloscope as follows:

- 1) Set the signal generator to a 100Hz triangle wave, but amplitude $V_I = 0$.
- 2) Connect the signal generator to the input. Set the amplifiers for CH1 and for CH2 to 1.0V/cm.
- 3) Set V_{DD} to 4.0V.
- 4) Set display to XY mode. A small dot should appear on the screen. Adjust the CH1 and CH2 offsets the dot is 2.0 cm from the upper left corner both in the X and Y directions. This point will correspond to $V_I = 0$ and $V_O = 4.0\text{V}$. Confirm these voltages with your fiducial scale.
- 5) Omit the jumper wire of figure 9A-1 until further notice. If left in place it will inflict a voltage spike on the V_O vs V_I curve trace.

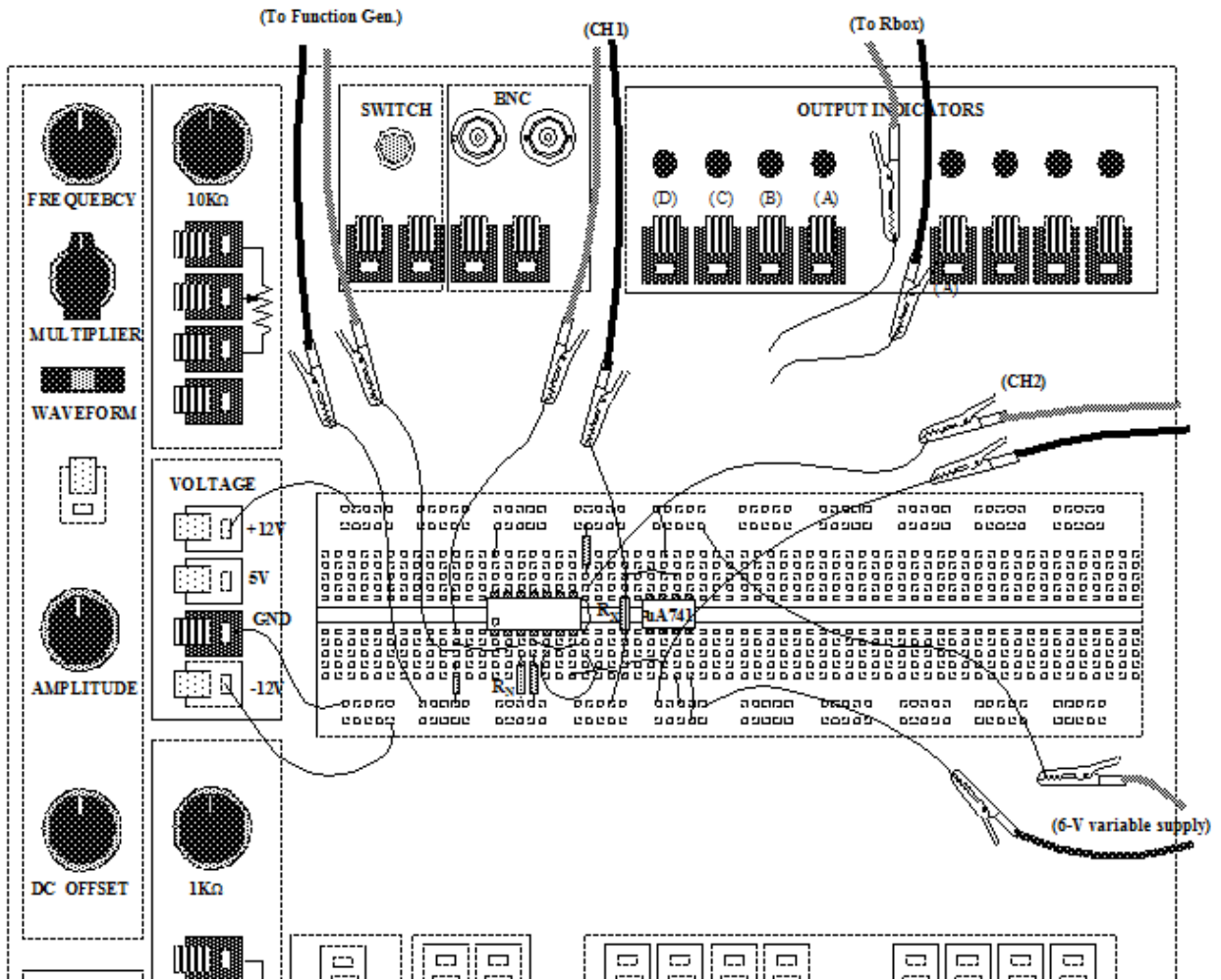


Figure 9A-2a. Suggested placement and wiring for figure A-1.

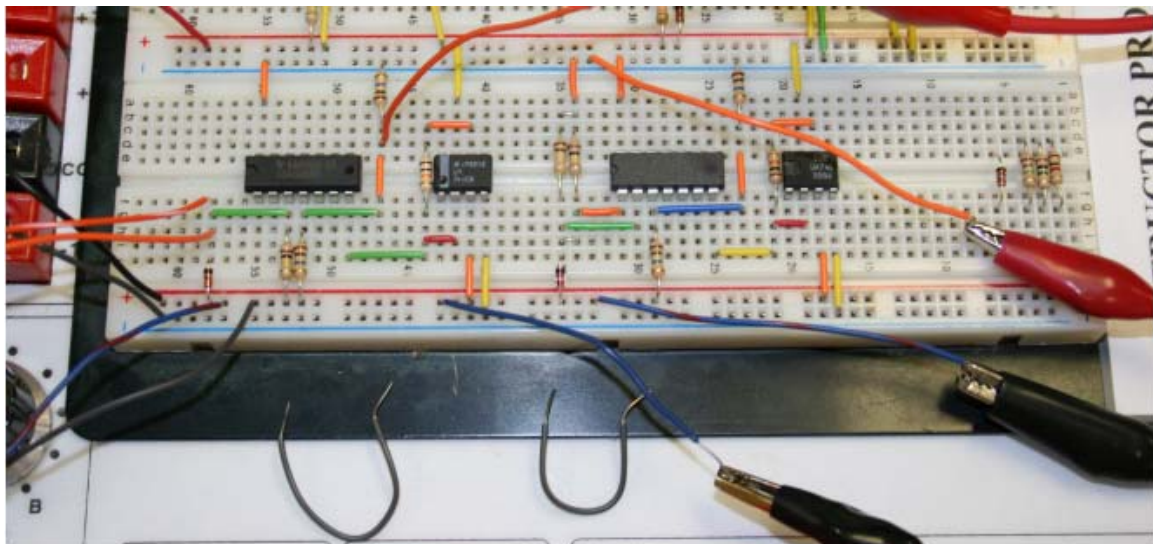


Figure 9A-2b. Photo of suggested placement and wiring for figure A-1 and for figure C-1. Jumper wires are not connected and are otherwise displaced.

A-3: Increase amplitude V_I which should bring up a V_O vs V_I trace not unlike that shown by figure 9A-3a. Adjust frequency of the triangle wave for best visibility and minimum hysteresis.

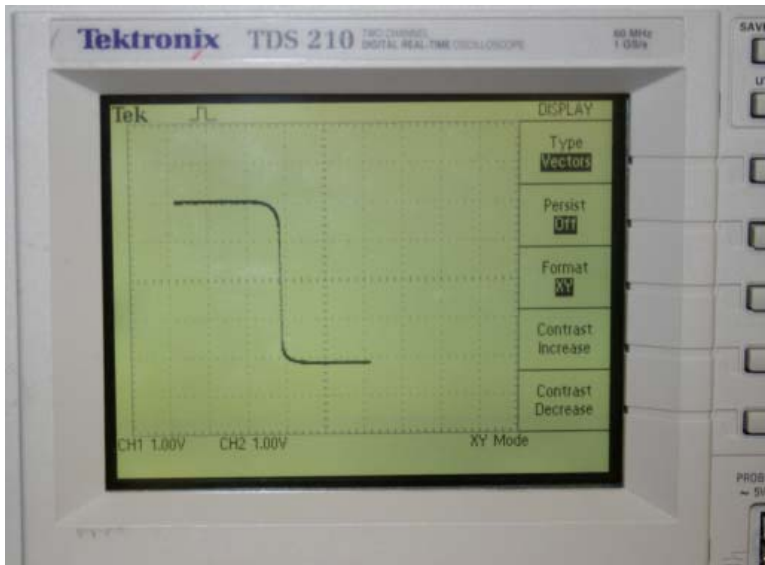


Figure 9A-3a. Photo snapshot of transfer curve V_O vs V_I for CMOS inverter.

For your measurements extract the logic benchmarks as shown in figure 9A-3b, i.e. determine values of (V_{ILM} , V_{IHm} , V_{OHm} , V_{OLM} , V_{IT1} , V_{IT2}) from this curve trace. It will be necessary to use your fiducial scales and the V/cm amplification of your O-scope CH1 amplification to do so. Keep in mind that each measurement must be referenced to the $V_I = 0$ point, so when/if you change amplification on CH1, also reduce V_I back to zero to find the $V_I = 0$ point. Then increase V_I until the V_O vs V_I trace re-appears. The cycle should give you assurance of a good set of valid measurements.

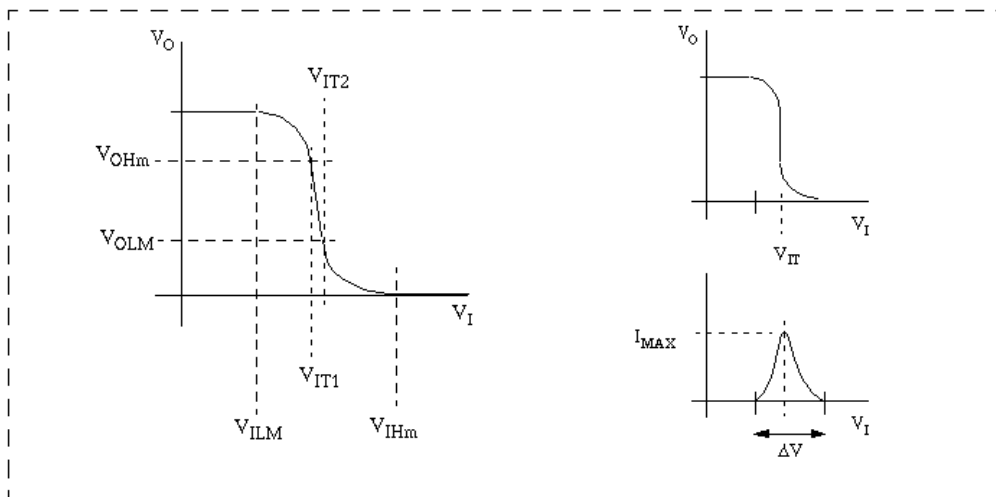


Figure 9A-3b: Transfer curve benchmarks

A-4. Now toggle the X-Y mode to the Y-T mode. The CH1 and CH2 traces will appear as separate $V(t)$ traces, as shown by figure 9A-4 and you can now use the cursors. Set cursors to reference time, and measure the same information as obtained by step A-3 except via the time scale fiducial axis. Measure the $\Delta V/\Delta T$ rising slope of the triangle wave as part of your calibration data. Make use of the 'Delta' interval measurement function of the (two) cursors. The same caveats applies as for the measurements for part A-3. Note that initialization for measurement is at the launch edge of the triangular wave shape (at which $V_I = 0$).

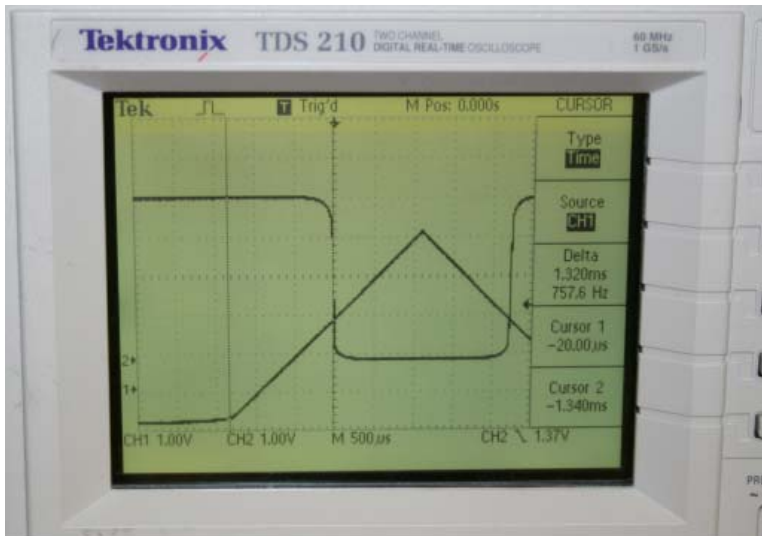


Figure 9A-4. Transfer curve traces on the X-T scale. Stabilize the o-scope traces by setting the trigger mode of the Oscoppe to CH2, falling edge.

Expand the time scale as necessary to obtain an improved measure of the CMOS transition regime. You might also try to correlate these to the X-Y measurements of V_{IT1} and V_{IT2} .

A-5. Move the output sampling node for CH1 from V_X to V_{X2} . An inverted profile of the transition current profile will appear on the Y-T scale, as shown by figure 9-A5. Adjust gain of CH2 and CH1 as necessary for good measurement of peak current I_{MAX} and profile width ΔV of the transition current. These measurements will appear as a ΔV_{X2} on the Y-scale and as a Δt on the time scale, respectively and will have to be translated into current and voltage (respectively) via your spreadsheet. Make good use of your fiducial scales and your cursors. Be aware that $I_{MAX} = \Delta V_{X2} / R_X$, and that $\Delta V = \Delta t \times m$, where $m = \text{slope of triangle wave}$. The peak of the current profile corresponds to V_{IT} . Include this value as a well-defined data measurement of V_{IT} for (later) comparison to equation (9-2a). V_{IT} should also be equal to $(V_{IT1} + V_{IT2})/2$.

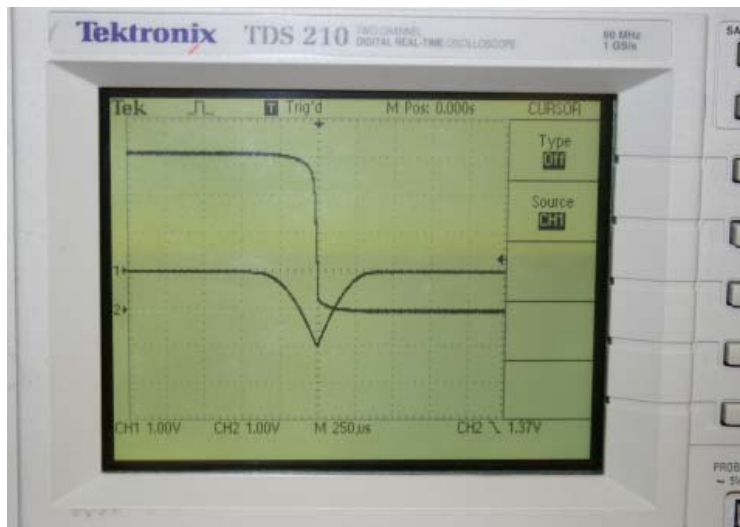


Figure 9A-5. The upper trace = CH2, and represents the CMOS transfer curve trace. The lower trace is CH1 and represents the transition current profile, inverted by the opamp output. The traces are stabilized by setting the trigger mode to CH2 falling edge, same as part A-4.

A-6. Repeat the measurements of parts A-3 thru A-5 for settings of $V_{DD} = 3.0V$, $5.0V$, and $6.0V$. The amplitude of the triangle wave sweep should also be re-adjusted as needed.

B-1. With $R_2 = 10M\Omega$, replace R_1 by the *Rbox* set to $9,999,999\Omega$ (or highest alternate 999... setting if $9,999,999\Omega$ is not available). Reset V_{DD} to $4.0V$. Connect V_I to V_{DD} (for which $V_O = \text{low} = 0.0V$).

Now adjust the *Rbox* decade by decade, and then more carefully until the output is pulled up to the value $0.5V_{DD}$. Record this value of resistance as R_{X1} . This value represents the (1/conductance) of the pull-down (nMOS) transistor when $V_{GS} = V_{DD}$ ($= 4.0V$, this instance). Set up a second data table (Excel data table #2) to record this value along with a record of the supply voltage.

B-2. Now interchange the measurement process of part B-1, for which $R_1 = 10M\Omega$ and R_2 by a resistance box set to $9,999,999\Omega$. Connect V_I to GND for which output = high = V_{DD} . Adjust the *Rbox* until the output is pulled down to the value $V_{DD}/2$ and record this value of resistance as R_{X2} . This value of R_2 represents the (1/conductance) of the pull-up (pMOS) transistor at $V_{GS} = 0.0$. Add this value of resistance to data table #2.

B-3. Repeat parts B-1 and B-2 for power supply rails at $V_{DD} = 3.0V$, $5.0V$, and $6.0V$ and include this information in your Excel data table #2.

C-1. Reconstruct the test setup by replacing the hex inverter with a CMOS NAND gate configured as an ‘inverter’, as represented by figure C-1. Note that the inputs are both connected to the upper rail by pull-up resistances (also reflected by the photo figure 9-2b). Check appendix for pin-out configuration of the NAND gate.

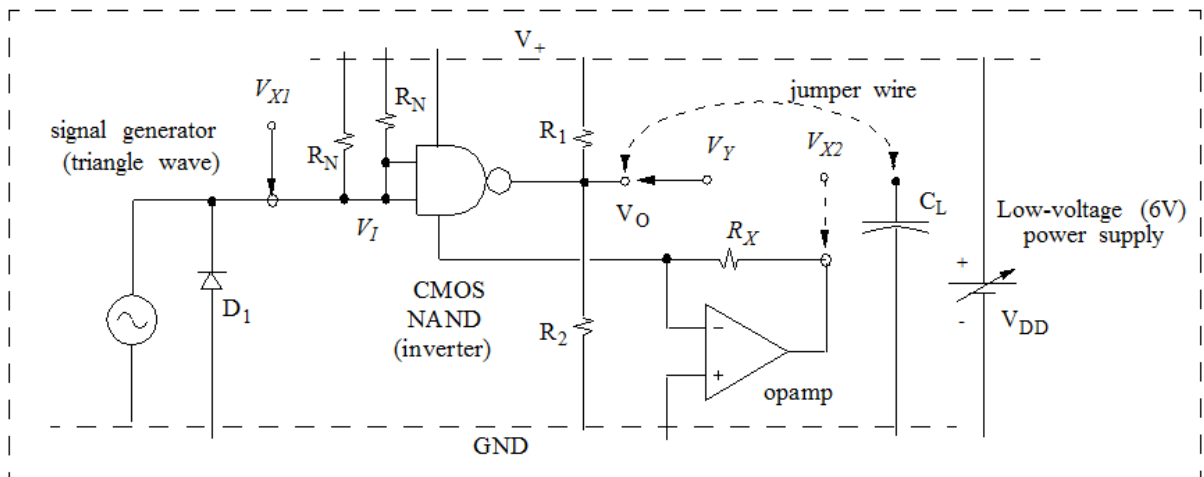


Figure C-1: Test set-up for evaluation of CMOS NAND/inverter transfer characteristics. It is topologically similar to the test setup of figure A-1 with exception of input resistance(s) R_N . Let $R_N = 100k\Omega$ and $R_X = 10k\Omega$, same as used for the tests made on the CMOS inverter.

C-2. Repeat the same measurement sequence for transfer curve characteristics as was conducted under parts A-2 through A-6, and record this data under a new Excel data table. You are almost repeating part A except with a CMOS NAND gate as an ‘equivalent’ CMOS inverter. Your transfer curves and current impulse should not look all that different from those of figures 9A-3a, 9A-4, and 9A-5, except skewed.

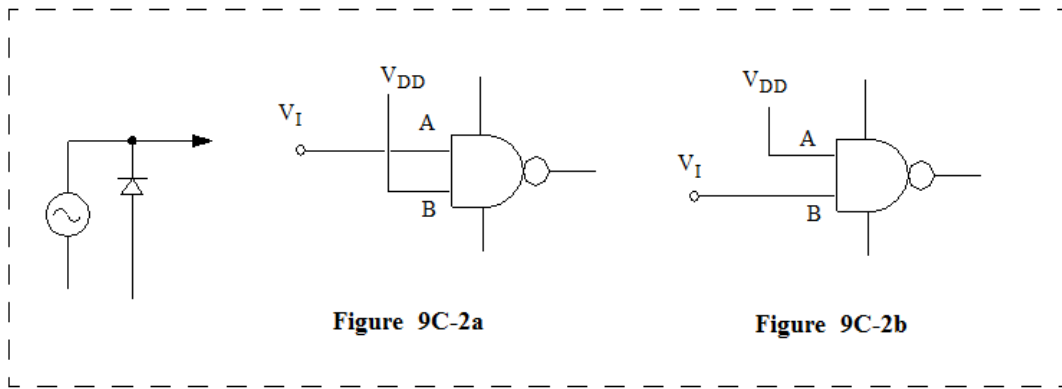


Figure 9-C2: Other equivalent inverter topologies for the NAND gate.

C-3. Repeat the measurement process of part C-2 for the equivalent NAND inverter topology as given by figure 9-C2a. This topology can be accomplished by a simple jumper wire, since the resistance path R_N forms a default pull-up.

C-4. Repeat the same measurement process for the equivalent NAND inverter topology represented by figure 9-C2b

ANALYSIS:

A. Using your Excel spreadsheet and the data as extracted for V_{ILM} , and V_{IHm} to identify values for V_{TN} and V_{TP} from the transfer curve data. (No plot, just correlation)

B. Create X-Y Excel plots as follows:

(a) V_{IT} ($= [V_{IT1} + V_{IT2}]/2$) vs V_{DD} and use the extracted values of V_{TN} and V_{TP} to compare the measurement data to equation (9-2a) and use curve-fitting to fit a value of K_R to the data.

VILM =	V _{TN}	0.6 V	(previous meas.)
-(V ₊ -V _{IHm}) =	V _{TP}	-0.9 V	(previous meas.)
	K _R	1.2	
Experiment			
	V _{IT}	V _{IT} (equation)	
	(V)	(V)	
V _{DD}			
3	1.3	1.3158	
4	1.8	1.7931	
5	2.2	2.2703	
6	2.9	2.7475	

Adjust K_R for best fit of equation to data

Example analysis: part B (a)

(b) I_{MAX} vs V_{DD} . Use the measured value of ΔV and the value of K_R obtained under part B(a) to ascertain K_N and K_P for the transistors. (Once again) be aware that $I_{MAX} = \Delta V_{X2}/R_X$, and that $\Delta V = \Delta t \times m$, where m = slope of triangle wave. Let your spreadsheet do the calculations for you.

(c) R_{X1} vs V_{DD} and align the data with $R_N = (0.5V_{DD})/I_D$ with I_D given by equation (9-1b) and V_{GS} set to be $= V_+$ ($= V_{DD}$) as was done by the measurements. Use curve-fitting to fit values of K_N (or β_N) and V_{TN} to this data. These fit-extracted values of V_{TN} and K_N should not be inconsistent with the same values found by parts A and B(b).

(d) R_{X2} vs V_{DD} and align the data with $R_N = (0.5V_{DD})/I_D$ with I_D given by equation (9-1b) with $V_{GS} = GND$. Use curve-fitting to fit values of K_P (or β_P) and V_{TP} . The fit-extracted values of V_{TP} and K_P should not be inconsistent with the same values found by parts A and B(b).

B. Using your Excel spreadsheet and the data as extracted for I_{MAX} and ΔV make X-Y plots of this information vs V_{DD} and compare this data to formulae (9-2a) and (9-2b). Use curve-fitting techniques to fit values of V_{TN} and V_{TP} using the values of K_N and K_P obtained under parts B(c) and B(d).

C. Plot the slope $\Delta V_{out}/\Delta V_{in}$ and compare to (9-2c) $I = I(V_{in} = V_{IT})$ and ΔV as given by (9-2b) and identify value for $V_{A1} = V_{A2}$ as curve-fitting parameters.

D. For the data extracted from the CMOS NAND versions of an inverter make plots of

- (a) V_{IT} vs V_{DD}
- (b) I_{MAX} vs V_{DD}

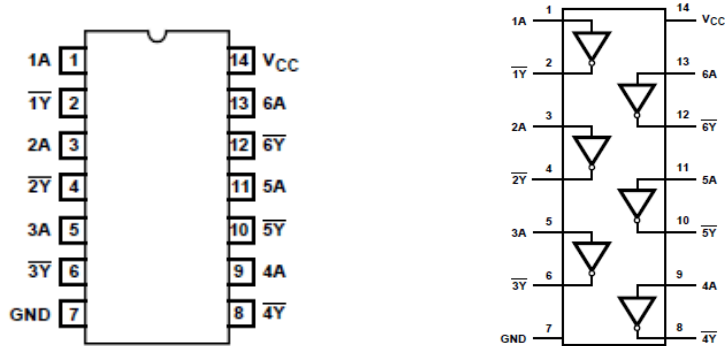
How do these compare to those of the analysis parts A and B? Identify skew factor for each by means of $V(skew, each) = V_{IT}(each\ case) - 0.5V_{DD}$.

You will have many plots (approx 12). Keep them small and concise and correlate with extracted results.

APPENDICES: Parts needed for this experiment are

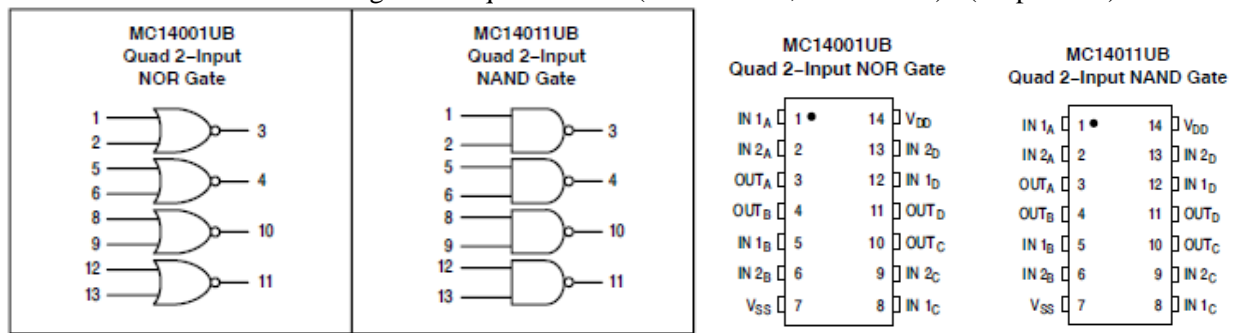
1 ea	CD4069UBE	CMOS Hex Inverter	3-18V
1 ea	MC14011UBCPG	CMOS NAND	3-18V
1 ea	741C opamp		

APPENDIX A-1: Pin-out diagram for (14-pin DIP) Hex inverter.



Data sheet URL for the CD4069UBE CMOS Hex Inverter is <http://focus.ti.com/lit/ds/symlink/cd4069ub.pdf>

APPENDIX A-2: Pin-out diagram for quad NAND (and/or NOR, if available) (14-pin DIP).



The data sheet URL for the MC14011UBCPG CMOS NAND is http://www.onsemi.com/pub_link/Collateral/MC14001UB-D.PDF

APPENDIX A-3. Pin-out for 741C opamp

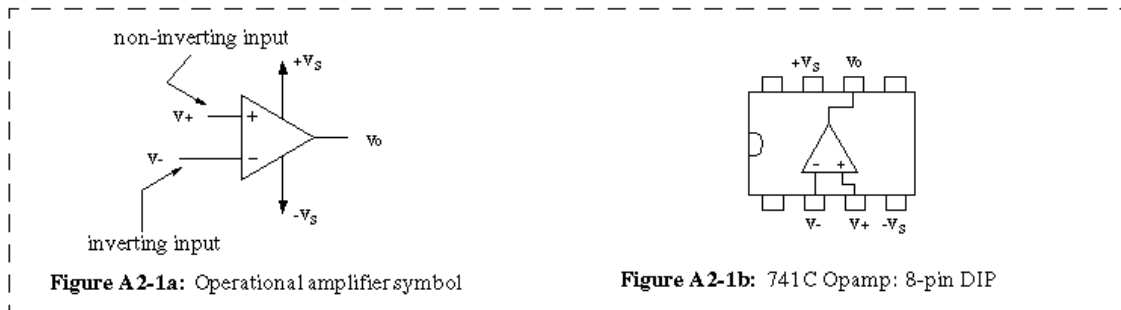


Figure A-2-1a: Operational amplifiersymbol

Figure A-2-1b: 741C Opamp: 8-pin DIP