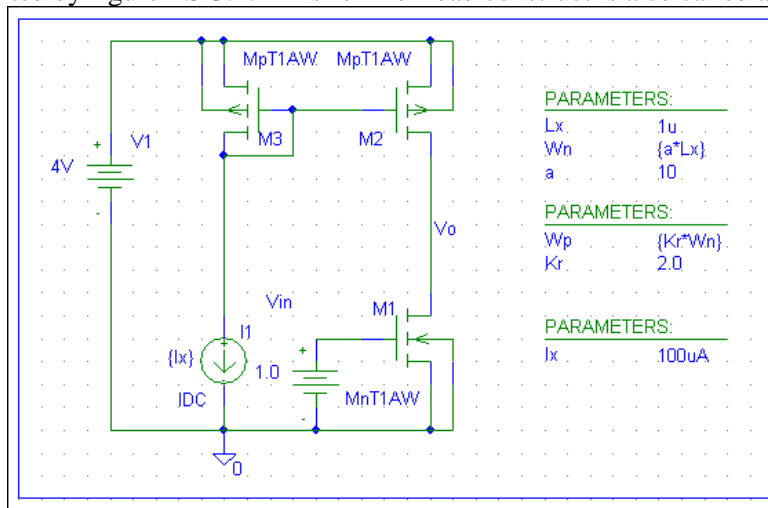


ECE8223      Exercise ES-3:      Transistor gain and small-signal analysis      vers1.3

**ES-3** One of the basic forms for an analog IC construct is the one for which a drive transistor is applied to a passive load. For circuits using discrete components, the load is usually a resistance. For analog IC design, the load is usually a transistor, and typically is of the form of a current source as represented by figure ES-3.1. This form of load construct is also called an *active load*.



**Figure ES-3.1:** Common-source configuration, active load, nMOS driver.

In the circuit shown, transistor M1 is the drive transistor and M2 is the active load. Transfer gain, as defined by the transition slope and small-signal analysis is of the equation form

$$v_o / v_{in} = \frac{dV_o}{dV_{in}} = - \frac{g_{m1}}{g_{DS1} + g_{DS2}} \quad (\text{ES-3.1})$$

where  $g_m = \sqrt{2\beta I}$  and  $g_{DS} = I/V_A$  for which  $\beta$  is the *conduction coefficient* of the drive transistor and  $V_A$  is the *Early voltage* for the transistor in question. These are called the *Level-2* forms.  $V_A$  must be obtained from curve fits to a set of I-V plots, as represented in a previous exercise (Exercise ES-2).

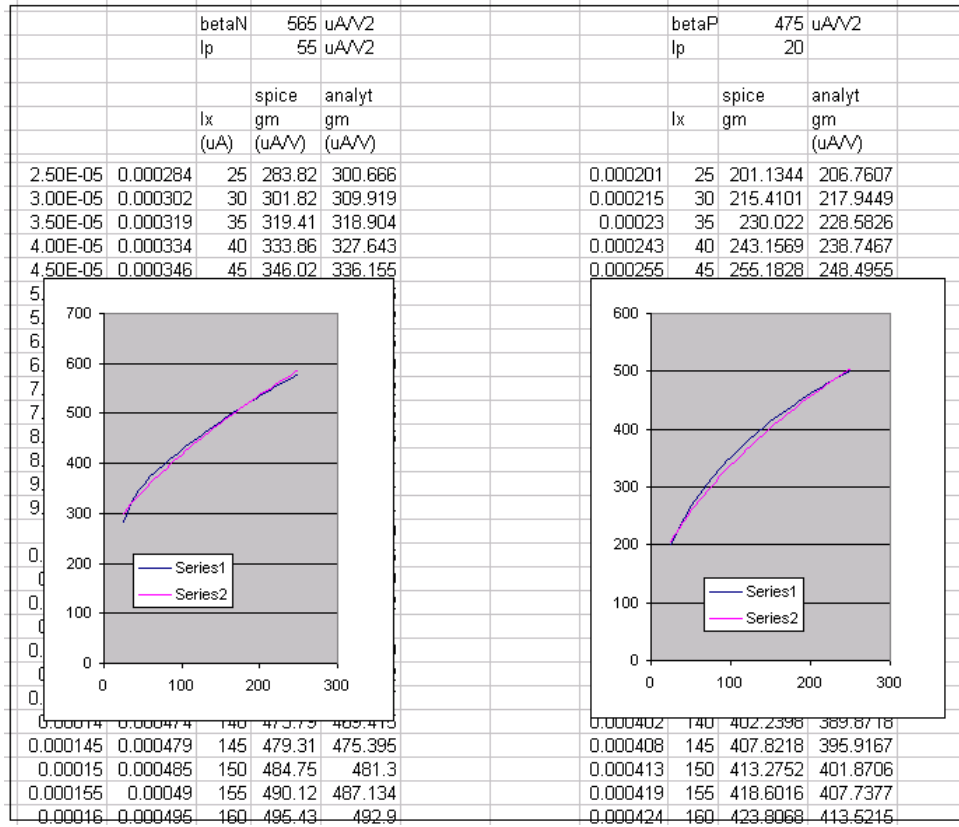
For higher technology situations equation (ES-3.1) is still OK, but the equations for small-signal (differential) parameters ( $g_m$  and  $g_{DS}$ ) are not. In fact it is appropriate to make (first-order) curvefits as follows:

$$g_{DS} = (I_o + I) / V_A \quad (\text{ES-3.2a})$$

$$g_m = \sqrt{2b_1\beta(I_1 + I)} \quad (\text{ES-3.2b})$$

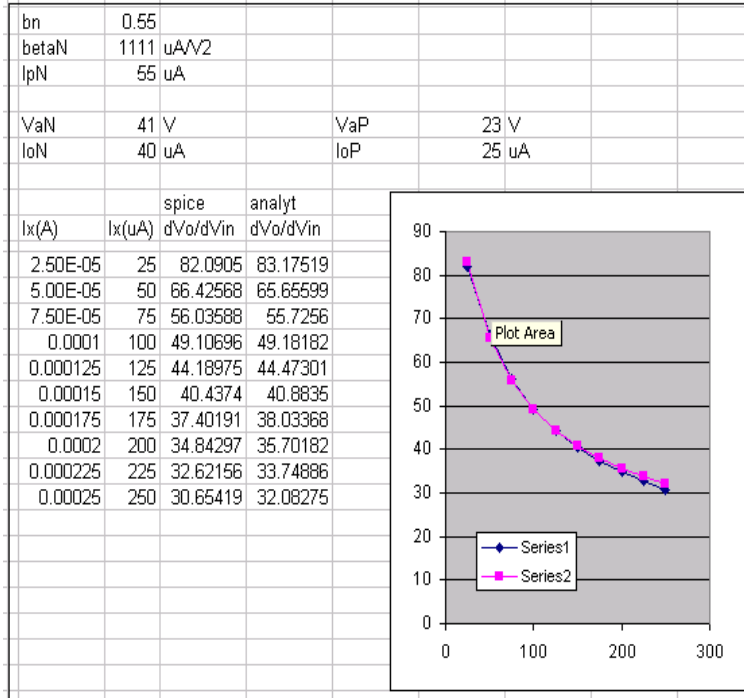
This may be accomplished by using the pSPICE/Excel process as used in exercise ES-2. In fact, in this exercise you should have actually fitted the analytical form of equation (ES-3.2a) to pSPICE plot of  $dI/dV_{DS}$  vs current  $I$ , so there is no need to repeat. In order to do the same analysis for  $g_m$ , it is necessary to fit equation (ES-3.2b) to a pSPICE plot of  $dI/dV_{GS}$  vs current  $I$ .

The ES-2 results should have looked something like figure ES3.2 (which was also run in class).

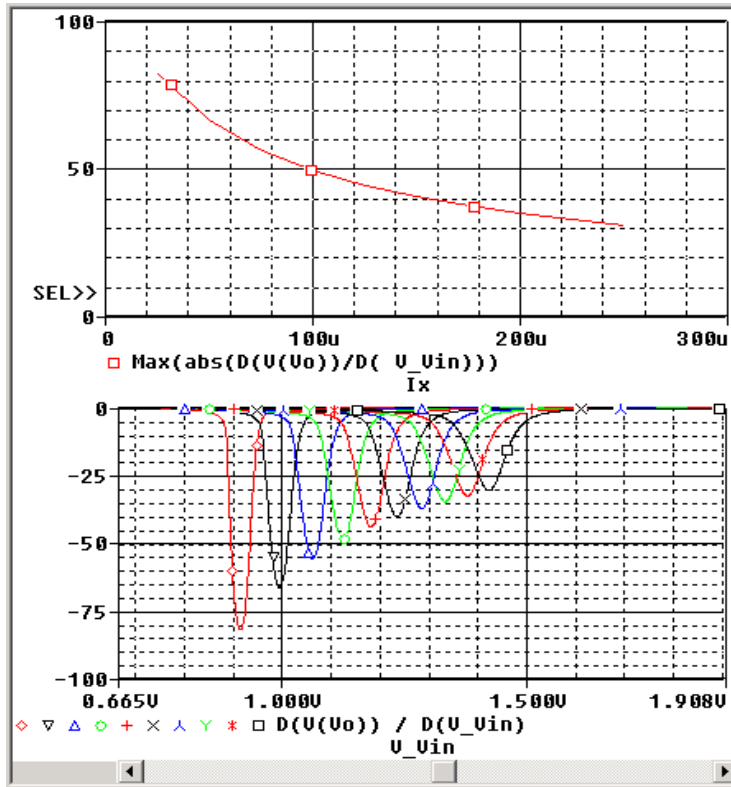


**Figure ES-3.2:** Fitting of equation ES-3.2b to pSPICE level-49 transistor behavior

Once  $g_m$  and  $g_{DS}$  fits have been accomplished, the results, when applied to equation (ES-3.1) are fairly reasonable, as shown by figure ES-3.3. The pSPICE data is that of  $dV_o/dV_{in}$ , for the peak slope in the transition region, as represented by figure ES-3.4.



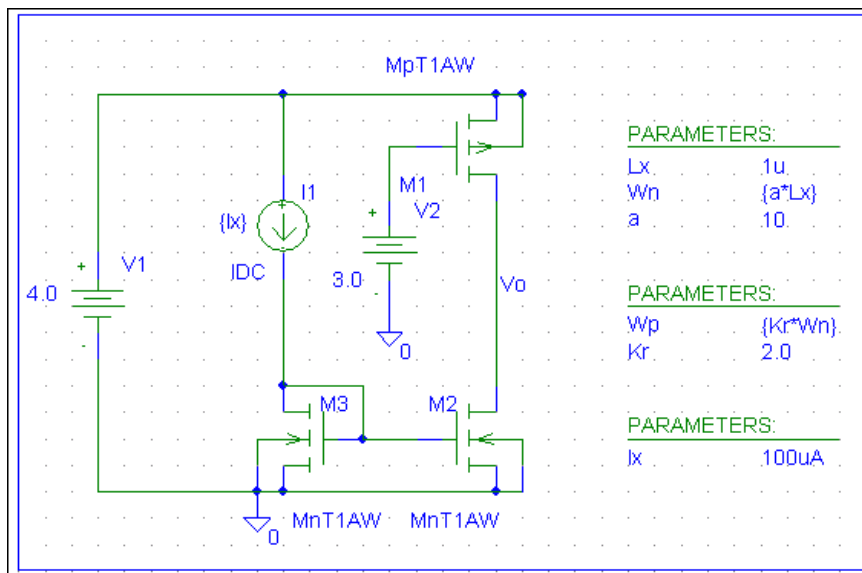
**Figure ES-3.3:** Comparison of  $v_o/v_{in}$  as generated by pspice to equation (ES-3.1), for which fittings of equations (ES-3.2a) and (ES-3.2b) are applied.



**Figure ES-3.4:** pSPICE response,  $dV_o/dV_{in}$ , vs  $I$ , and using schematic of figure ES-3.1, for T1AW parameters and level-49 device model.

**Requirement:**

- (a) Using this discussion as a template repeat this analysis but for Mosis process VO1V. You should have four figures, which you should label as *your* figures ES-3.1, ES-3.2, ES-3.3, ES-3.4. The template indicates all of the necessary constructs. The execution does rely on you having accomplished an expertise with the pSPICE and Excel utilities through the previous exercises. Your end result (figure ES-3.4) should be fairly good. If it is not, make a snake check. This figure will be the focus of the review done by the professor.
- (b) Repeat part (a) but for the circuit of figure ES-3.5 (pMOS version of figure ES-3.1). You should only need three figures, inasmuch as figure ES-3.2 should cover both circuits. Change figure numbers appropriately.



**Figure ES-3.5:** Common-source configuration, active load, pMOS driver.