

ES-4 The signature output characteristic of a current source or active load is its output conductance G_{out} . Ideally $G_{out} = 0$. For the simple current mirror (single transistor) $G_{out} = g_{DS}$. Output conductance G_{out} can be considerably reduced by means of a techniques in which transistors are stacked in the form called ‘cascode’.

The test topology for evaluation of the cascode current mirror is shown by figure ES-4.1. The purpose of the test is to evaluate the output conductances for the nMOS and pMOS versions of this topology and compare them to their theoretical values as given by equation (ES-4.1).

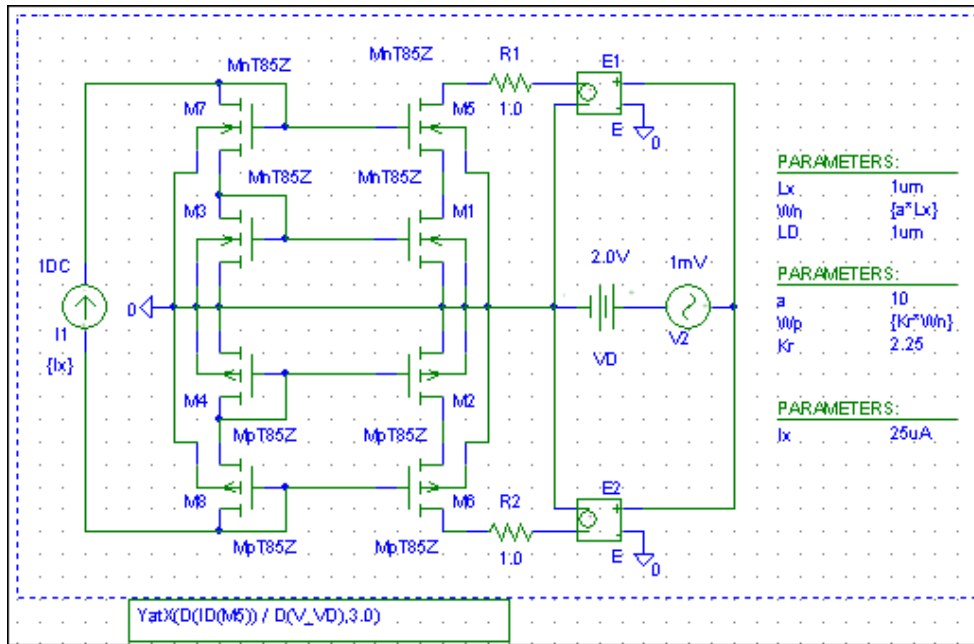


Figure ES-4.1: Test circuit for nMOS and pMOS cascode current mirrors.

In the circuit shown, transistors M1 and M5 form an nMOS cascode pair and transistors M2 and M6 form a pMOS cascode pair. The transistors are biased by a like pair of transistors which also serve as the means for passing reference current I_x to the cascode pairs under test.

Output conductance G_{out} (nMOS version) is determined by small-signal analysis as

$$G_{out} = g_{DSN} g_{DSN} / g_{mN} \quad (\text{ES-4.1})$$

where $g_{mN} = \sqrt{2\beta_N I}$ and $g_{DSN} = I/V_{AN}$ for level-1 analysis for which β_N is the conduction coefficient and V_{AN} is the Early voltage for the transistor(s) in question. For the advanced technology and level-49 model V_{AN} must be obtained from curve fits to a set of I-V plots, as achieved in a previous exercise (Exercise ES-2).

For higher technology situations equation (ES-4.1) is still OK, but the equations for small-signal (differential) parameters (g_m and g_{DS}) are not. It appropriate to make use of first-order curvefits for which:

$$g_{DS} = (I_o + I_x) / V_A \quad (\text{ES-4.2a})$$

$$g_m = \sqrt{2\alpha_1 \beta (I_1 + I_x)} \quad (\text{ES-4.2b})$$

as realized from the pSPICE/Excel exercise ES-2.

The principal problem of dealing with high-performance circuits as represented by figure ES-4.1 is that they will push the limits of your simulation software. You will likely have to readjust the iteration limit of the numerical analysis. For pSPICE the numerical settings are located under the **Analysis > Setup > Options** menu. The parameter that will most likely need to be adjusted is the RELTOL (relative tolerance) setting. It is suggested that you choose a value a few orders of magnitude smaller than the default .001 such as RELTOL = 1.0u. Depending on the convergence factors of the topology and device models the smaller tolerance should only mildly slow the iteration.

Sweep V_D from 0 to 4.0V and step the current setting I_x through the same range as used in exercises ES-2 for which conductances g_{DS} and g_m were evaluated. This should result in a family of curves from which the performance analysis plot of G_{out} for the nMOS cascode pair can be extracted. The nMOS result is represented by figure ES-4.2. The macro $\text{YatX}(,)$ should be used to accomplish this assessment. Execute this macro for both $V_{DS} = 2.0$ and $V_{DS} = 3.0$ (The second argument of the macro)

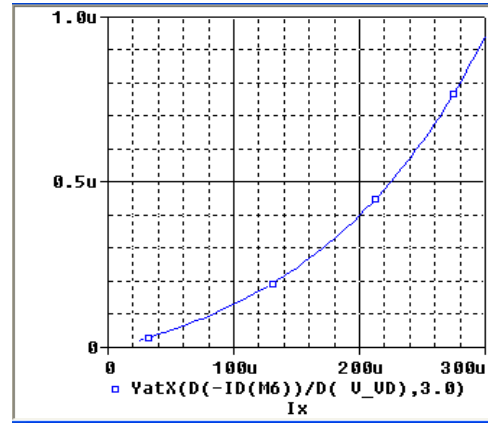
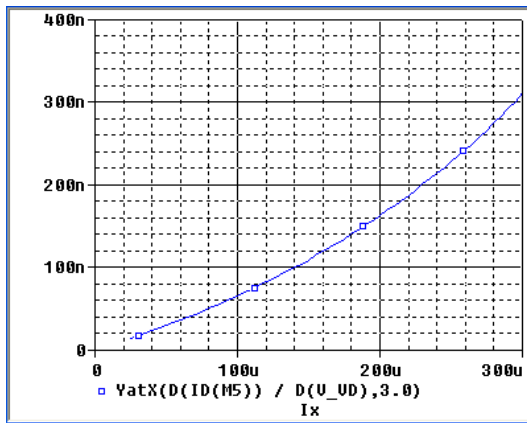


Figure ES-4.2a. G_{out} for nMOS cascode mirror. **Figure ES-4.2b.** G_{out} for pMOS cascode mirror.

For the higher voltages, the G_{out} starts to increase as consequence of higher-order field effects. But it is still very low and less than $1\mu\text{A/V}$.

Now import your pSPICE data for G_{out} vs I_x into the (Excel) spreadsheet that was generated for conductances g_{DS} and g_m and compare to the analytical equation (ES-4.1). Results should be comparable in magnitude but not necessarily a good fit since cascoding invites contributions from some additional terms.

Requirement:

- (a) Apply this analysis to MOSIS process VO1V. You should have two figures labeled as figures ES-4.2(a) and ES-4.2(b) for the nMOS and the pMOS cascode topologies, respectively, showing comparisons between the two pSPICE executions and the analytical equivalent.

Also include a figure that shows your test schematic, as figure ES-4.1.

- (b) Show comparison between analytical and the pSPICE outputs for $V_{DS} = 3.0\text{V}$ in like manner as part (a). Label these figures as ES-4.3(a) and ES-4.3(b) for the nMOS and pMOS cascade mirrors.