

ES-4 Another one of the basic forms for analog IC constructs is the high-performance cascode current mirror. The nMOS topology for the cascode current mirror is given by figure ES-4.1

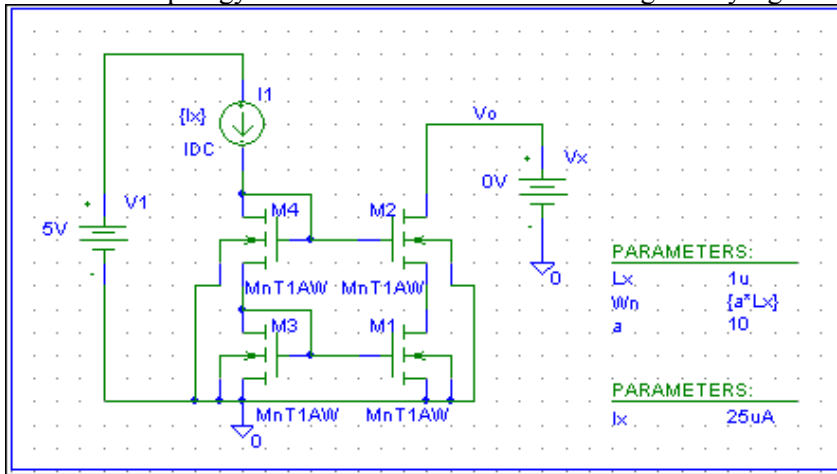


Figure ES-4.1: nMOS cascode current mirror.

In the circuit shown, transistors M1 and M2 form a cascode pair. Output resistance R_{out} and compliance ΔV are the performance parameters of interest. Output resistance is given by small-signal analysis

$$R_{out} = r_{DS1}(g_{m2}r_{DS2}) \quad (\text{ES-4.1})$$

where $g_{mN} = \sqrt{2\beta_N I}$ and $g_{DSN} = I/V_{AN}$ for which β_N is the *conduction coefficient* of the transistor and V_{AN} is the *Early voltage* for the transistor in question. These are called the *Level-1* forms. V_{AN} must be obtained from curve fits to a set of I-V plots, as represented in a previous exercise (Exercise ES-2).

For higher technology situations equation (ES-4.1) is still OK, but the equations for small-signal (differential) parameters (g_m and g_{DS}) are not. It appropriate to make (first-order) curvefits for which:

$$g_{DS} = (I_o + I)/V_A \quad (\text{ES-4.2a})$$

$$g_m = \sqrt{2b_1\beta(I_1 + I)} \quad (\text{ES-4.2b})$$

This may be accomplished by using the pSPICE/Excel process as used in exercise ES-3. But in fact, in this exercise you should have actually fitted the analytical forms of equations (ES-4.2a) and (ES4.2b) to pSPICE plots. So there is no need to repeat.

The principal problem of dealing with high-performance circuits, as represented by figure ES-4.1 is that it will push the limits of your simulation software, and most likely you will have to readjust the numerical analysis iteration parameters. For pSPICE, the key numerical settings are located under the **Analysis > Setup > Options** menu. And the most likely setting that will need to be adjusted is the RELTOL (relative tolerance) setting. For best results, you should probably choose something a few orders of magnitude smaller than the default setting .001, such as RELTOL = 1.0n. But the smaller the tolerance (usually) the slower the iteration.

For this circuit you should expect to sweep V_x from 0 to 5.0V and step the current setting I_x through a reasonable range, such as 25uA to 250uA, step 25uA. This should result in a nice family of curves for $R_{out} = d(V(Vo))/d(ID(M2))$. (Figure ES-4.2a). A “performance analysis” plot of the maximum level of R_{out} is indicated by Figure ES-4.2b

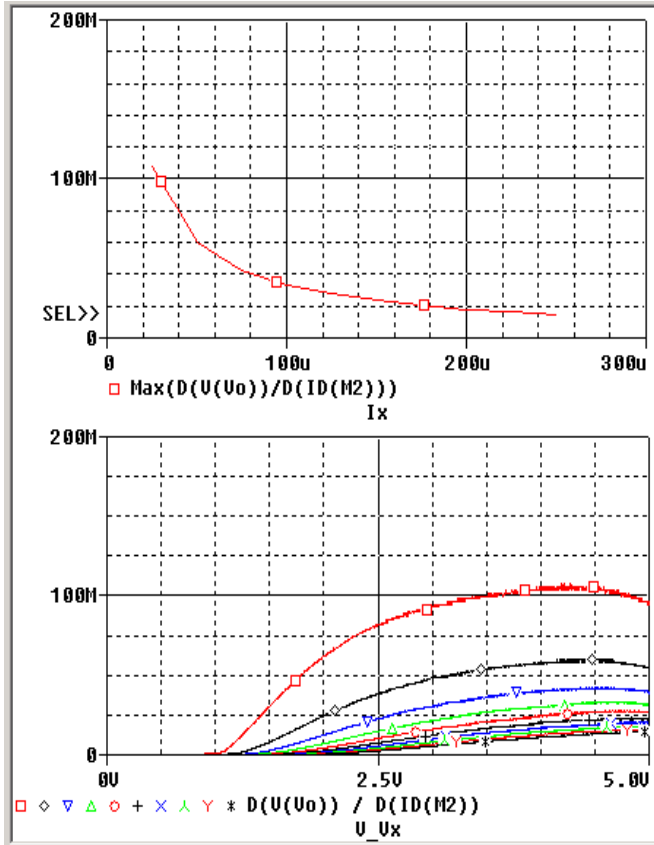


Figure ES-4.2: R_{out} for cascode mirror.

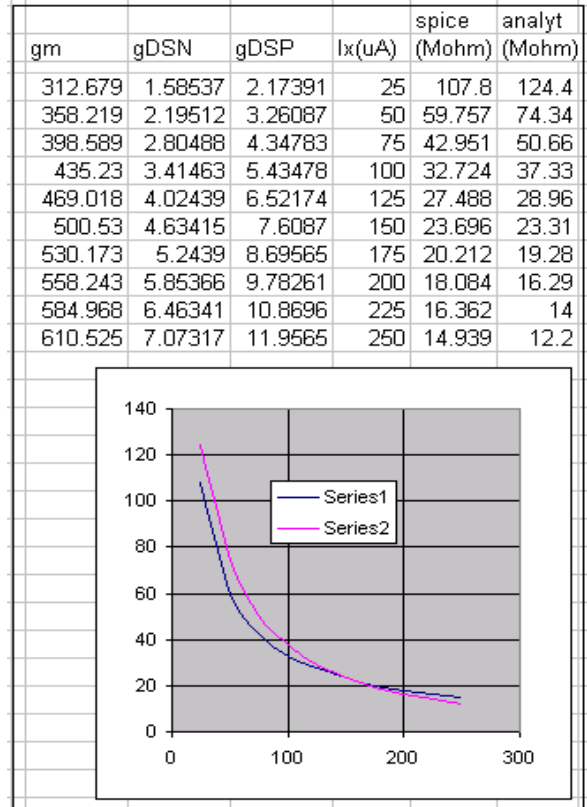


Figure ES-4.3: Comparisons: pSPICE R_{out} vs analytical R_{out}

For the higher voltages, the R_{out} starts to diminish as consequence of higher-order field effects. But it is still very high, on the order of 10-100M Ω .

Now import your pSPICE data for $R_{out}(max)$ vs I_x (figure ES-4.2b) into the (Excel) spreadsheet and compare to the analytical results of using equations (ES-4.2a) and (ES-4.2b) with equation (ES-4.1). Results should be comparable, as represented by figure ES-4.3. A little timesaving can be achieved by making use of the same spreadsheet as was used for exercise ES-3 (which determined g_{DS} and g_m). You should save the “new” file under a different name so as to not lose the previous information.

Requirement:

- (a) Using this discussion as a template repeat this analysis but for MOSIS process T77Z. You should have three figures, which you should label as *your* figures ES-4.1, ES-4.2, ES-4.3. The template indicates all of the necessary constructs. The execution does rely on you having accomplished an expertise with the pSPICE and Excel utilities through the previous exercises. Your end result (figure ES-4.3) should be fairly good. If it is not, make a snake check. This ending figure will be the focus of the review process.
- (b) Repeat part (a) but for the circuit of figure ES-4.4 (pMOS version of figure ES-4.1). Change figure numbers appropriately.

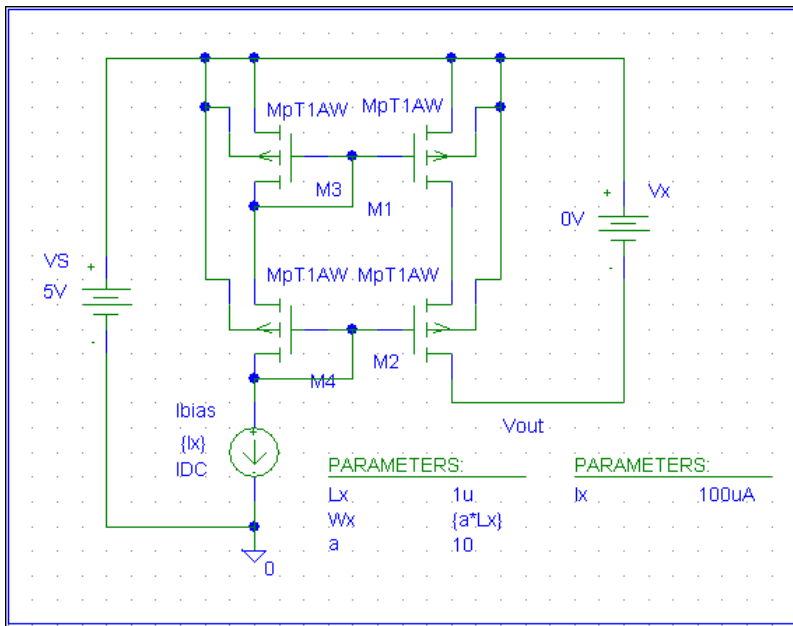


Figure ES-4.4: Cascode current mirror, pMOS version