Mississippi State University
ELECTRICAL AND COMPUTER ENGINEERING

ECE 4263/6263
Principles of VLSI Design

OBJECTIVES

By the end of this course, the student will be able to

Physical Electronics and FET Operation

- outline and explain the levels in the VLSI design abstraction pyramid,
- define basic terminology of physical electronics, e.g. carrier, semiconductor, donor, acceptor, intrinsic, extrinsic, etc.,
- explain subthreshold operation, Fowler-Nordheim tunneling, drain punch through, and the hot electron effect,
- explain the fundamental operation of NFETs and PFETs in their three modes of operation, the effect of basic FET parameters on FET operation, and the body effect,
- apply the ideal FET equations to determine a FET's operating region and solve FET circuits, and
- apply simplified FET models and calculate equivalent resistance and transistors for FETs.

CMOS Processing

- outline the steps in CMOS processing including (a) forming ingots, (b) creating wafers, (c) growing oxides, (d) doping methods, (e) using photoresist and etchant, (f) forming gate/drain/well regions, (g) "lightly doped drain" devices, (h) creating interconnects, and (i) planarization,
- explain the difference, advantages, and disadvantages of N well, P well, twin tub, and SOI processes
- explain the processing and use of additional metal layers, local interconnections, special capacitance poly, trench capacitors, high resistance and thin-film layers, and floating gates,
- explain the physical CMOS processing reasons behind specific design rules,
- interpret specific design rules and apply them in creating a DRC "clean" layout, and
- explain the "latchup" phenomena, how it is triggered, and how it can be prevented.

CMOS Inverter

- define and explain the significance of CMOS inverter (logic gate) basic terminology, e.g. threshold voltage, noise margins, rise/fall time, propagation delay
- derive and explain the detailed operation of a CMOS inverter in its five operating regions,
- derive and apply the CMOS inverter analysis and synthesis design equations,
- design a CMOS inverter to have specific static and switching characteristics, and
- optimize CMOS inverter behavior and performance by varying transistor gain factor, capacitance, power supply voltage, and FET dimensions.

CMOS and TG Logic Gates

- calculate a FET network's input/output relationship or the necessary gate signals to give a desired FET network input/output relationship,
- design an efficient FET network to perform a logic function,
- explain the operation of NFET, PFET and CMOS TGs,
- calculate the function performed by NFET, PFET, and CMOS TG networks,
- design a NFET, PFET, and CMOS TG network to perform a logic function,

- describe/draw the circuit topology of basic logic gates (NAND, NOR, XOR, tristate inverter, latch, D-FF, multiplexer, etc),
- explain the basic logic gate operation, and
- select and justify logic circuit topology given a set of design objectives.

Circuit Parameter Estimation

- identify mechanisms that create resistance in circuit design,
- calculate estimation for interconnect and transistor resistances,
- design an interconnect to have a specific resistance using the material's sheet resistance, and via properties,
- explain the MOS capacitor operation during accumulation, depletion, and inversion,
- identify causes of parasitic capacitances,
- calculate estimation for interconnect and transistor parasitic capacitances,
- design an interconnect to have a specific resistance using the material's sheet resistance, and via properties,
- explain "ground bounce" and how to mitigate its effects,
- explain how parasitic resistances and capacitance limit circuit performance,
- estimate circuit delays using a simple RC and distributed RC models,
- determine the geometries that allow routing resistance and capacitance to be ignored, and
- design a "super" buffer circuit to drive large capacitive loads with minimum delay.

Physical Design and Layout

- explain the advantage of and apply Euler paths to find efficient gate ordering for physical design,
- interpret a stick diagram and its constituent components,
- create the stick diagram for a given circuit design, and
- optimize a gate's physical design (stick diagram) for maximum performance, and explain each optimization.

Device Sizing

- determine the analytic analysis/synthesis design equations for an arbitrary CMOS logic gate,
- outline and explain the method of equivalent inverter gate design,
- calculate an estimate of threshold voltage and rise/fall times using the equivalent inverter method,
- design a logic gate for threshold voltage or rise/fall time using the equivalent inverter method,
- outline the procedure for calibrating and using the logic effort design method,
- explain the role of each parameter in the logical effort design method,
- derive the expression for optimum stage effort and number of stages to achieve minimum delay,
- derive the logical effort and parasitic delay for arbitrary logic gates, derive the electrical effort for arbitrary circuits/applications,
- design logic gate FET widths for minimum delay, and
- evaluate candidate logic gate circuit topologies within their electrical environment.

System Design

- justify the choice of standard cell versus fully custom ASIC design methods,
- describe and estimate the static and dynamic power dissipation in a CMOS circuit,
- outline and explain the top-down/bottom-up design flow, outline and explain the circuit design flow, and
- explain design margining methods, yield, and the use of corner models.