ECE 4743 – Digital System Design

Course Objectives: By the end of the course, you should be able to do the following things:

- **Combinational, Sequential, and Structural VHDL.** Write a textual description of a digital schematic which can be compiled and downloaded into a configurable chip. Designs can be used modularly to minimize design time and maximum reuseability.

- **Implementation Technologies.** Identify target implementations given design guidelines and constraints. Determine which design tool is most appropriate to use for a given design (VHDL, Verilog, Schematic Capture).

- **Datapath Design & Control.** Given a datapath, select and design a control mechanism (FSM, Microcode). Given an equation or process, design a dataflow graph. Then design a datapath following the constraints of the system or problem definition.

- **System Timing.** Determine worst-case scenarios for timing delays given a specific design. Minimize the worst-case using good design techniques (pipelining, scheduling, registering I/O).

- **Testing & Evaluation.** Given a design, create a test program to check for opens and shorts.