MISSISSIPPI STATE UNIVERSITY

Department of Electrical & Computer Engineering

Ph.D. Qualifying Examination — Fall 2012

Code Number:_____

1. All wireless devices must be turned off for the duration of the exam.
2. The duration of the exam is 4 hours (8:30 am–12:30 pm).
3. Each student is provided with a folder that includes a total of 25 problems. Including this instruction sheet, you should have a total of 30 pages. Check to ensure that you have a complete exam.

   Note: Problems 8, 9, 16, and 23 are two pages each

4. This exam is closed book and closed notes. No reference material is allowed. A basic calculator is permitted.
5. Blank sheets are available as needed. Do not write on the backside of any sheets.
6. Your code number must appear on every sheet, including this instruction sheet and any additional sheets that you may use. **Do not write your name or student ID on any of the sheets.**
7. You must choose 8 problems (a minimum of 2 problems from upper-level courses) for grading. Keep all pages of each problem together; place the problems to be graded into the rings in the center of your folder. **Circle in the grid below the problems that you are turning in for grading.**
8. Turn in your folder, which includes in the rings this instruction sheet and the 8 problems that you select. Place all other materials, included the other problems, into the side pockets of the folder. **You are not allowed to take any of the exam pages from the room.**

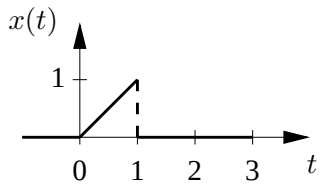
Problem Number

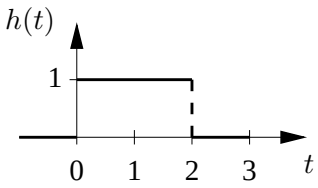
ECE Core:	1	2	3	4	5	6	7	8	9	10	11	12	
ECE Upper Level:	13	14	15	16	17	18	19	20	21	22	23	24	25

Code Number _____

Problem 1 (ECE Core)

Consider the continuous-time signals below.





Find $y(t) = x(t) * h(t)$ for $-\infty < t < \infty$.

Code Number_____

Problem 2 (ECE Core)

A parallel plate capacitor C_o (plate area = 10 cm^2, plate separation = 2 mm) is filled with a dielectric material characterized by $\sigma = 10^{-8}$ mho/m and $\varepsilon_r = 6$.

(a.) The equivalent circuit for this capacitor consists of an ideal parallel plate capacitor C in parallel with an ideal resistor R. Determine R and C.

(b.) Determine the magnitude of the total charge on either capacitor plate when a voltage of 12 V is applied to C_o.

(c.) Determine the total conduction current through the dielectric of C_o when a voltage a 12 V is applied.

(d.) If the voltage source is disconnected from C_o, how long will it take the total charge found in (b.) to decay to one tenth of its original value?

Code Number_____

Problem 3 (ECE Core)

An antenna produces the following far field phasor magnetic field in spherical coordinates (r,θ,ϕ):

$$H_\phi = \frac{2}{r}\sin\theta\cos\phi\ e^{-jkr} \quad (A/m)$$

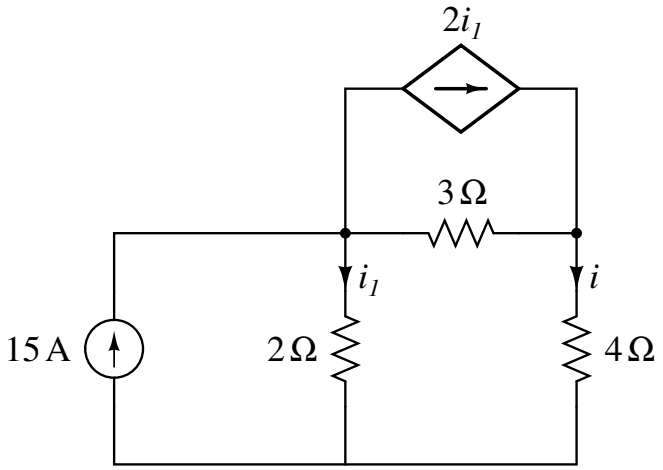
Determine

(a.) the time-average vector power density in the far field.
(b.) the total radiated power.
(c.) the antenna radiation resistance.

Code Number _____

Problem 4 (ECE Core)

Find i in the circuit below.



Code Number_____

Problem 5 (ECE Core)

A single - phase, 20 kVA, 2400/240 V transformer has the following parameters:

$R_1 = 4.0\ \Omega$; $R_2 = 0.04\ \Omega$; $R_{c1} = 35\ k\Omega$

$X_1 = 5.0\ \Omega$; $X_2 = 0.05\ \Omega$; $X_{m1} = 4.0\ k\Omega$

The transformer is supplying its rated current to a load at 240 V and 0.8 pf leading.

a) Draw the *approximate equivalent circuit* of the transformer, showing values of the elements to the primary side

b) Determine the input voltage of the transformer V_1 = _____ V

c) Calculate the transformer voltage regulation VR = _____ %

d) Find The core loss, copper loss and efficiency of the transformer P_{core} = _____ W

P_{cu} = _____ W

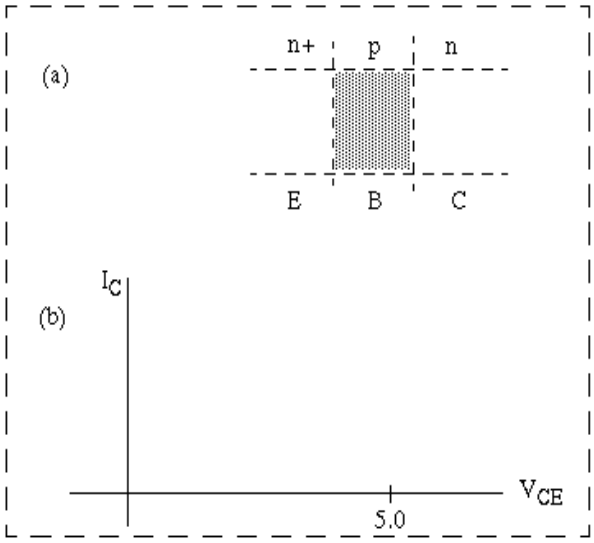
η = _____ %

e) Draw the phasor diagram showing all voltage and currents

Code number _____

Problem 6 (ECE core)

***npn* transistor**



(a) Indicate on the slice across the transistor (figure)
(1) the direction (arrow) of the collector electric-field.
(2) the flow of electrons and

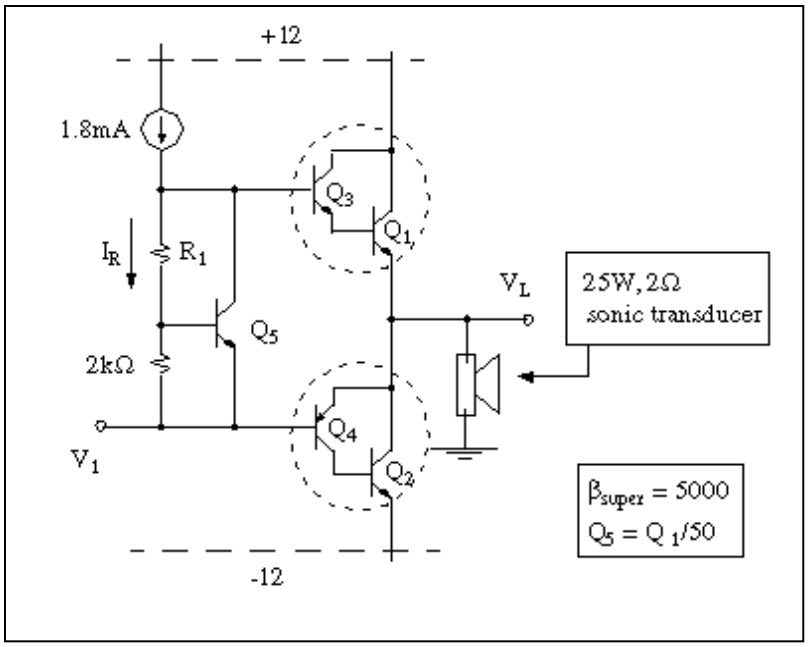
(3) the necessary junction biases (use +, - to indicate) for the BJT to be in the active mode.

(b) (1) Sketch a reasonable plot of a family (each trace due to a different values of I_B) of the output characteristics I_C vs V_{CE} characteristics of the *npn* transistor for $0 < V_{CE} < 5.0$V. (2) indicate the slopes (pointer) for which the Early voltage V_A is defined.

Code number _____

Problem 7 (ECE core)

Power amplifier stage: For the circuit shown, I_{bias}, V_S (non-optimized) and R_2 are specified. Assume junctions operate at V_J = 0.6V at quiescent conditions and using the specifications shown determine:



(a) $I_{B3}(max)$ = _____

(b) R_1 = _____

(c) $P_D(ckt, worst\ case)$ = _____

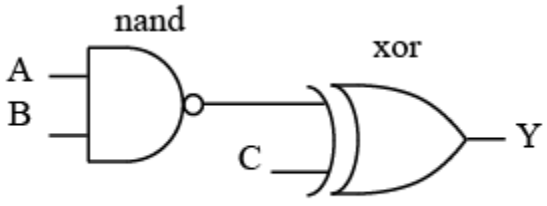
(d) I_R = _____

(e) *Max efficiency* = _____

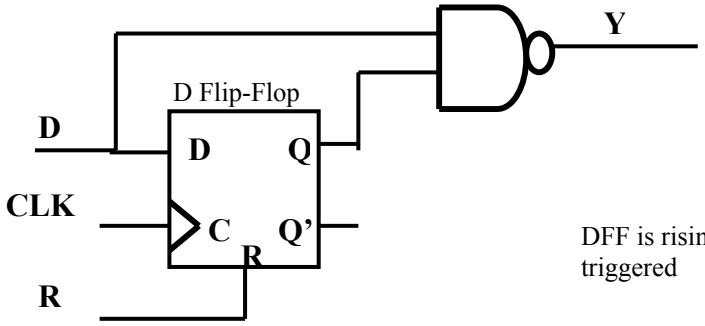
Code Number_____

Problem 8 (ECE Core)

A. Give the truth table of the logic network below:

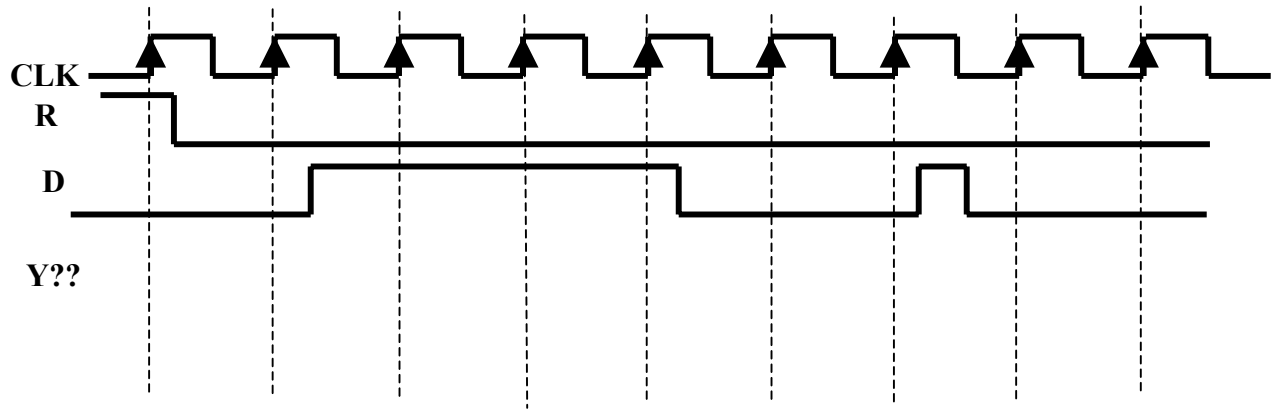


B. Complete the timing diagram for the Y output for all clock cycles.



DFF is rising edge triggered

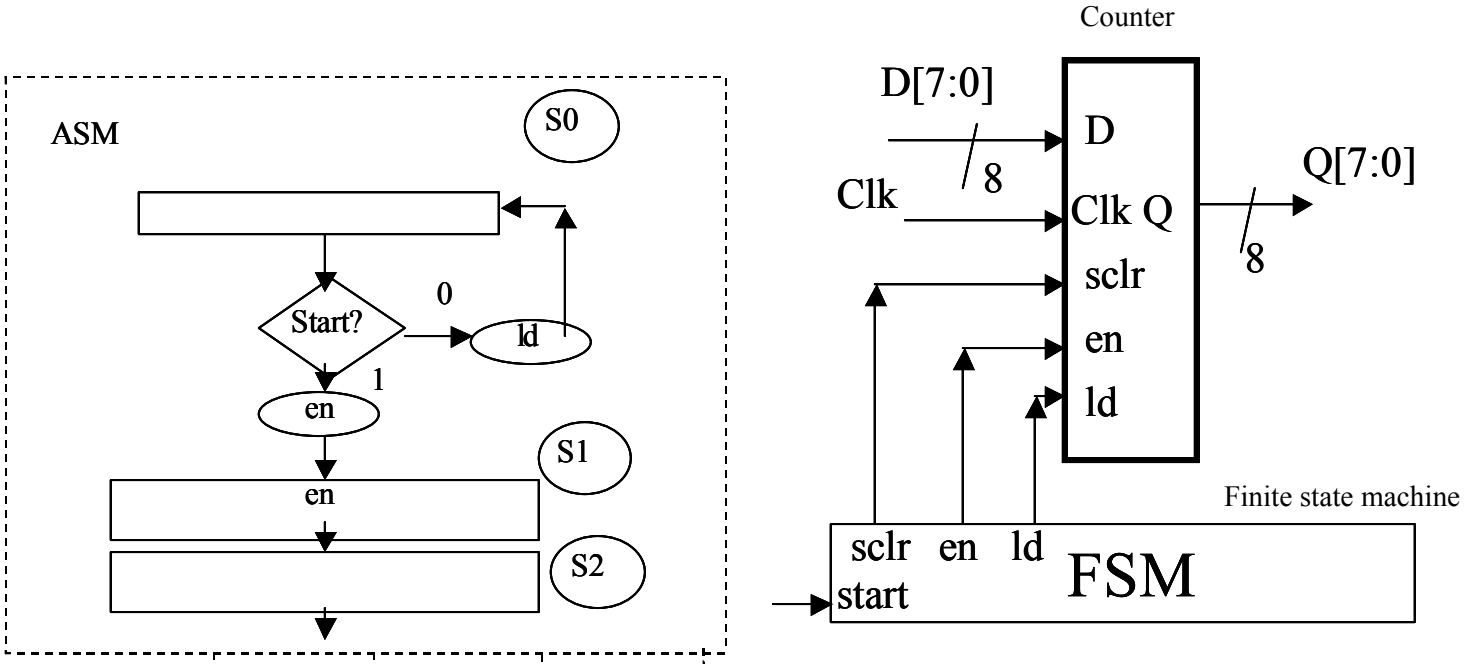
asynchronous reset, high-true

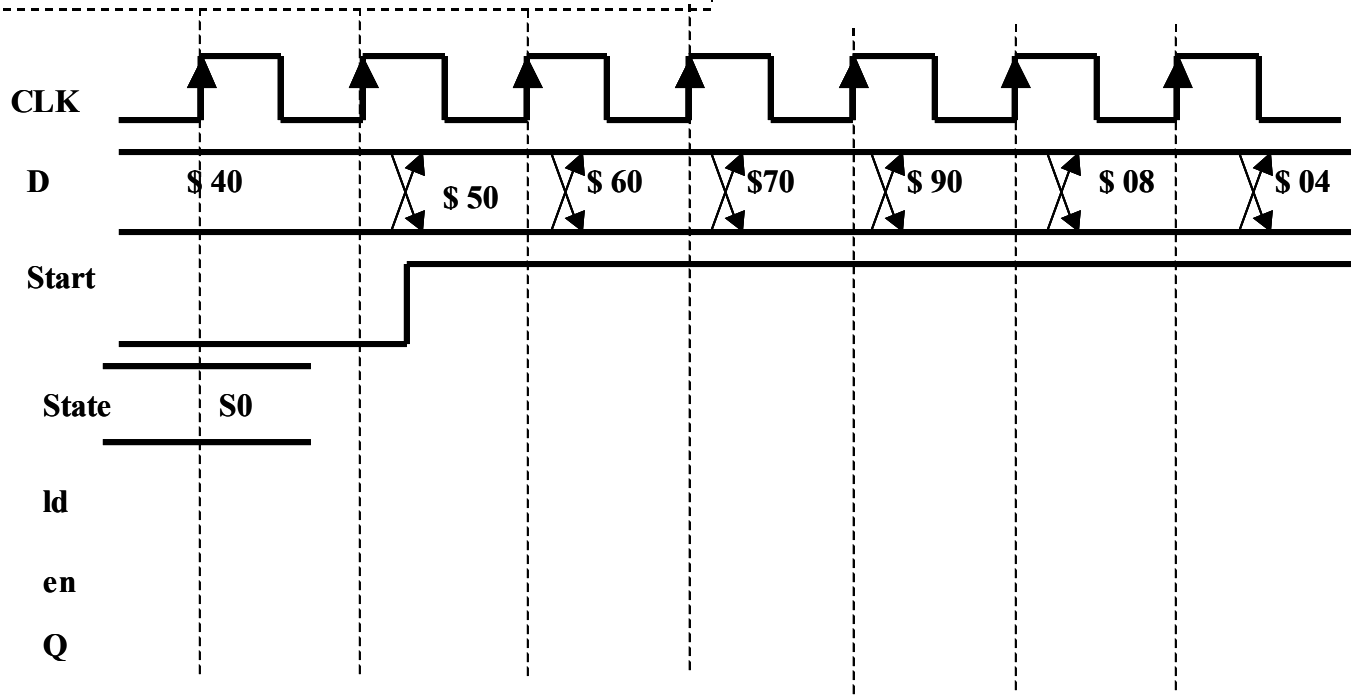


Code Number_____

Problem 8 (ECE Core)

C. The ASM chart below specifies the behavior for the finite state machine that is controlling the counter that is shown. On the timing diagram, fill out the waveforms for the State, ld, en, and Q values given the Start and D values shown. Draw the waveforms through state S2 of the ASM. Assume the counter and FSM are rising-edge triggered.





Counter behavior (ALL output changes occur on rising clock edge!)
When en is asserted, the counter counts up.
When ld is asserted, the counter loads from the D inputs.
When sclr is asserted, the counter is cleared.

If neither en, ld, or sclr is asserted, the counter holds the current value.

Code Number_____

Problem 9 (ECE Core)

Because PhD applicants have diverse microprocessor backgrounds, you are given an instruction set for a fictional microprocessor and asked questions about it. This fictional microprocessor instruction will change from PhD exam to PhD exam, do not assume that you will see the same instruction set as given below.

Assume a microprocessor with R0 thru R7 with 8-bit DATA registers. The processor also has A0 thru A3 16-bit ADDRESS registers. The processor has Z (zero), C (carry), N (negative, value of Most Significant Bit of result), and V (2's complement overflow) status flags. Multi-byte values are assumed stored in **little-endian** order in memory (Least Significant Byte first). All load and store operations move 8-bit values from/to memory. The address space of the processor is 16-bits.

Some instructions for this processor are

LDD 8-bit immediate, Rn 8-bit imm → Rn -- loads a 8-bit immediate into data register, no flags affected

LDA 16-immediate, An 16-bit imm → An -- loads a 16-bit immediate into address register, no flags affected

LEA Ax,n Ax + n → Ax -- loads the effective address Ax+n into Ax; n is an 8-bit 2's complement value, no flags affected.

LD [Ax,n], Rx [Ax+n] →Rx -- the contents of memory location [Ax +n] is loaded into register Rx. No flags affected. 'n' is an 8-bit 2's complement offset.

ST Rx, [Ax,n] Rx →[Ax+n] -- the contents of Register Rx is stored at memory location [Ax+n], no flags affected. 'n' is an 8-bit 2's complement offset.

TEST Rx,Ry Rx-Ry -- performs Rx-Ry for testing purposes, all flags are affected, no register contents are altered. Carry flag is set to '1' if no borrow occurs, Carry is cleared to '0' if borrow occurs.

ADD Rx,Ry Rx + Ry → Rx -- add operation, all flags affected

ADC Rx,Ry Cflag + Rx + Ry → Rx -- add with carry operation, all flags affected

SUB Rx,Ry Rx - Ry → Rx -- subtract operation, all flags affected. Carry flag is set to '1' if no borrow occurs, Carry is cleared to '0' if borrow occurs.

SBB Rx,Ry Rx – Ry – NOT(CFLAG) → Rx -- subtract with borrow operation, all flags affected

BZ address (branch on Z=1 to address); BNZ address (branch on Z=0 to address)
BC address (branch on C=1 to address); BNC address (branch on C=0 to address)
BV address (branch on V=1 to address), BNV address (branch on V=0 to address)
BN address (branch on N=1 to address), BNN address (branch on N=0 to address)
BRA address unconditional branch

Code Number_____

Problem 9 (ECE Core)

Question:
For the C code in the following questions, an 'int' is a 16-bit value (2 bytes), a 'char' is a 8-bit value (1 byte), and a 'long' is a 32-bit value (4 bytes). Multi-byte values are stored in little endian order, Memory is byte addressable (all addresses refer to byte values).

a. Write assembly code that implements the following C code fragment:

```
unsigned int p, k;

p = p - k;
```

Assume that the variables are stored beginning at location 0x100 in memory.

b. Write assembly code that implements the following C code fragment. Assume that P, Q are stored in memory beginning at location 0x100.

```
unsigned char P,Q;

if ( P >= Q)  {
        /// place holder for IF-BODY instructions do not implement
      }
```

Code Number_____

Problem 10 (ECE Core)

The intrinsic carrier concentration in a semiconductor material at room temperature is **$1x10^{10}$ cm^{-3}**.

The intrinsic carrier concentration in the same semiconductor material at 800°C increases to **$5x10^{16}$ cm^{-3}**.

This semiconductor was doped with an acceptor impurity.
The total concentration of the acceptors incorporated in the semiconductor is N_A=**$3x10^{15}$ cm^{-3}**.
The acceptors are shallow.
This semiconductor was also doped with a donor impurity.
The total concentration of the donors incorporated in the semiconductor is N_D=**$2x10^{15}$ cm^{-3}**.
The donors are shallow.

1) Is this material n-type, or p-type, or anything else at room temperature? Explain why.

2) Determine the value of the electron concentration (n) and hole concentration (p) in this material at room temperature.

3) Is this material n-type, or p-type, or anything else at 800°C? Explain why.

4) Explain why the intrinsic carrier concentration at 800°C is higher than at room temperature.

5) Determine the value of the electron concentration (n) and hole concentration (p) in this material at 800°C.

Code Number_____

Problem 11 (ECE Core)

a. In any programming language that you wish, define a data structure for a SINGLY linked list based on pointers and write a function that adds a new item to the end of list given any node in the list and the item to be added. Your code must be well-commented.

b. Describe how a max-heap (or min-heap) data structure functions (draw a picture to help your argument).

Code Number_____

Problem 12 (ECE Core)

Answer three of the following four questions:

1. **How many edges in a fully connected graph if the graph has:**

   a. **3 nodes** _____

   b. **7 nodes** _____

   c. **37 nodes** _____

   d. **100 nodes** _____

2. **If there are 25 students in a class and the professor wants to form 5 teams of 5 students each, how many different ways can this be done?**

3. **Given the following graph, determine the minimum spanning tree and the total weight of that MST:**

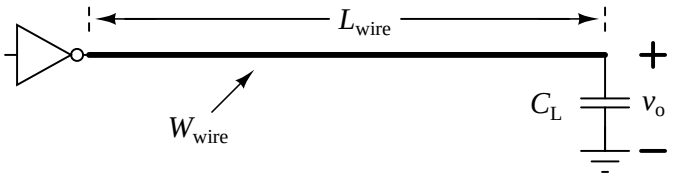
	a	b	c	d	e	f	g
a	0	3	1	2	0	0	6
b	3	0	4	5	1	1	1
c	1	4	0	2	3	0	2
d	2	5	2	0	0	0	4
e	0	1	3	0	0	0	3
f	0	2	0	0	0	0	1
g	6	1	2	4	3	1	0

4. **Recently, MSU started the Bulldogs in Motion program, and part of the requirement for successful completion of that program is that every member of each team must attend a training session in seven out of ten weeks. Each training session is offered twice per week. How many different ways can one person satisfy this requirement?**

Code Number _____

Problem 13 (ECE Upper Level)

The figure belows shows a CMOS inverter used to drive a load capacitance C_{L} over an interconnect with length L_{wire} and width W_{wire}. In this scenario, the time to charge/discharge C_{L} is τ_1.



Now assume the wire width W_{wire} is halved. C_{L} is unchanged. How is the new charge/discharge time τ_2 related to time τ_1 in the first situation? Justify your answer. Be specific.

(In engineering, clear communication of your ideas and reasoning is often more important than the actual numerical answer. Start good habits now. Use complete sentences, correct spelling and grammar.)

Code Number _____

Problem 14 (ECE Upper Level)

1. Do the following questions.

   1) How does performance relate to execution time in a formula?_____
   a. Performance = execution time
   b. Performance = execution time/10^6
   c. Performance = $10^6 \times$ execution time
   d. Performance = 1/ execution time

   2) Which one is not the MIPS addressing mode?_____
   a. Register addressing mode
   b. Indirect addressing mode
   c. Immediate addressing mode
   d. Base addressing mode

   3) Which one does not affect to improve CPI directly? _____
   a. Cache memory
   b. Pipeline
   c. Clock Rate (technology)
   d. Parallel execution

2. Assume that there are two machine implementations, M1 (500 MHz) and M2 (700 MHz), of the same instruction set. There are 5 classes of instructions for the *gcc* program and refer to the CPI and frequencies in the table below.

Instruction Classes	CPI on M1	CPI on M2	*gcc* Frequencies
Loads	4	4	25 %
Stores	3	4	10 %
Arithmetic/Logic	3	3	40 %
Branches	2	2	15 %
Jumps	2	3	10%

a) Compute the effective CPI on M1 and M2 when running the *gcc* program?

b) Compute the MIPS ratings on M1 and M2 when running the program?

c) The *gcc* program executes in 5 seconds for the machine M2. Then, how many instructions are executed when the *gcc* program is run?

Code Number_____

Problem 15 (ECE Upper Level)

In the space below, sketch the energy band diagram of a P-N-P bipolar junction transistor (pnp BJT) biased in the Active mode of operation (not cut-off or saturation).

Accurately label Emitter (E), Base (B), and Collector (C) regions.

For each of the E, B, and C regions, accurately label conduction band (E_C), valence band (E_V), Fermi level (E_F), intrinsic Fermi level (E_i), potential barriers between the two junctions (V_{EB} and V_{BC}).

Answer the following questions and provide explanation:

1) In the Base, which is higher, donor concentration or acceptor concentration?

2) Is the Emitter-Base junction forward biased or reverse biased?

3) Is the Base-Collector junction forward biased or reverse biased?

4) Considering the useful (desirable) component of the collector current, what type of carriers – electrons or holes - are responsible for that current? Where do they come from?

Code Number _____

Problem 16 (ECE Upper Level)

Given the equation $Y = (X*a_0) + (Z*a_1) + (X@2*a_2)$ and hardware constraints of one adder and one 3-stage pipelined multiplier,

a) Draw a dataflow graph, labeling all nodes, which can be scheduled in the minimum number of clock cycles.

b) What is the latency for this dataflow graph?

c) Schedule the operations for minimum clock cycles using the above constraints. (Note: not all clock cycles may be used in the table below)

	Multiplier	Adder	I/O
Clk N			
Clk N+1			
Clk N+2			
Clk N+3			
Clk N+4			
Clk N+5			
Clk N+6			
Clk N+7			

d) What is the percent efficiency (utilization) of the resources (the multiplier and the adder) of the previous schedule?

Code Number _____

Problem 16 (ECE Upper Level)
(continued)

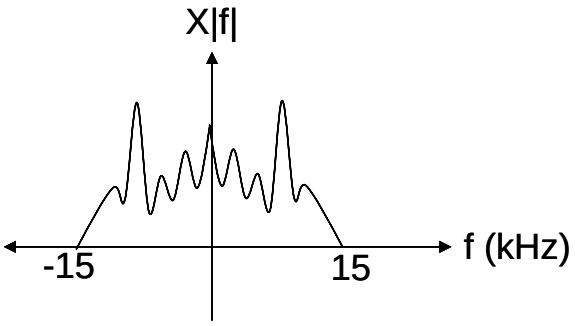
e) Give the generalized schedule of operations for minimum clock cycles using the above constraints and an **initiation rate of 2 over multiple samples**: Complete the table as much as possible.

	Sample J-1	Sample J	Sample J+1
Clk N-3			
Clk N-2			
Clk N-1			
Clk N			
Clk N+1			
Clk N+2			
Clk N+3			
Clk N+4			
Clk N+5			
Clk N+6			
Clk N+7			

Code Number: _____

Problem 17 (ECE Upper Level)

Consider an analog audio signal with the following spectral response:



Assume the analog signal is digitized using an A/D converter with the following specifications:
-sampling rate of 4fx, where fx denotes the Nyquist sampling frequency
-bipolar quantization with full range of 5volts and stepsize of 5/256volts
How much memory (in Megabytes) would be required to store a 5minute song?

Code Number: _____

Problem 18 (ECE Upper Level)

A triple-tone signal contains exactly three frequencies: 300Hz, 1000Hz, and 1200Hz. The signal is sampled at a rate of fs=4000Hz.

a) What is the smallest number of samples that could be collected in order to know for sure whether or not the 1000Hz component is present? Assume you are using a Rectangular window.

b) What is the minimum order of DFT that you could use to know whether or not all three frequency components are present? Again, assume you are using a Rectangular window.

c) Assume you use an FFT algorithm to compute your DFT. Which FFT coefficients will have the highest values if all three frequency components are present?

Code Number _____

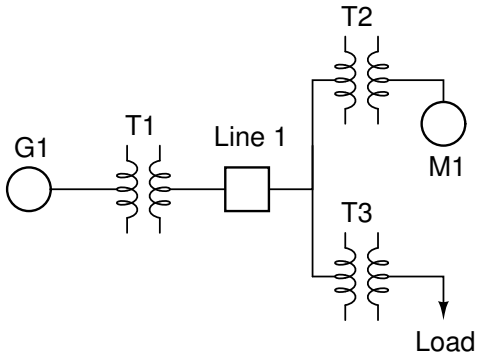
Problem 19 (ECE Upper Level)

For the three-phase system below, assuming a base at the motor of 13.2 kV and 125 MVA,

1. Calculate the $S_{base3\varphi}$, V_{baseLL}, and Z_{base} for each region;
2. Draw the per unit circuit diagram;
3. Calculate and label the per unit values on the circuit diagram.

HINT: $X_{pu}^{new} = X_{pu}^{old} * \left(V_{base}^{old}/V_{base}^{new}\right)^2 * \left(S_{base}^{new}/S_{base}^{old}\right)$

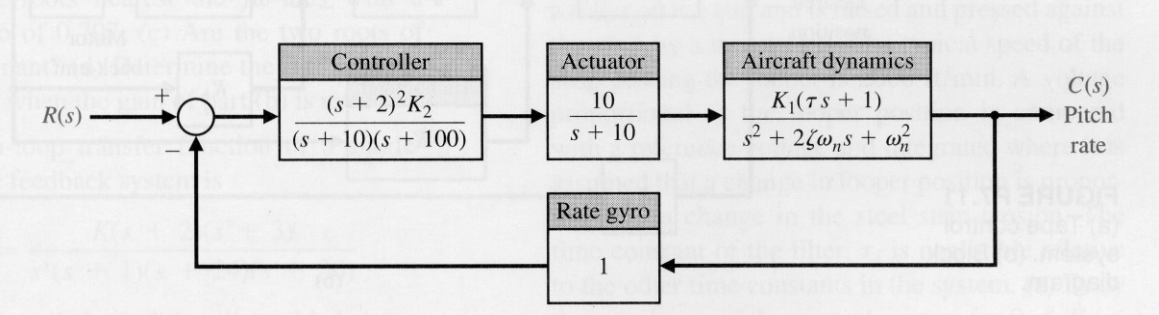
G1	13.2 kV, 120 MVA X = 3%
T1	13.8 kV/120 kV, 125 MVA X = 0.025 pu
Line 1	$\mathbf{Z} = 3 + j7$ ohms
T2	115 kV/13.2 kV, 150 MVA X = 5%
T3	115 kV/4800 V, 75 MVA $\mathbf{Z} = j0.03$ pu
M1	13.2 kV, 50 MVA X = 0.04 pu
Load 1	$\mathbf{Z} = 0.4\angle 18.19°$ ohms



Code Number _____

Problem 20 (ECE Upper Level)

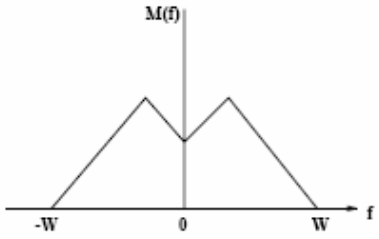
1. Given the block diagram below, which describes a hypothetical future supersonic passenger jet (to replace the Concorde), we would like to design the control system such that the vehicle has a compensated damping ratio of $\zeta = 0.7071$. The existing characteristics are that $\omega_n = 2.5$, $\zeta = 0.30$, and $\tau = 0.1$. A difficulty in this setup is that the gain factor K_1 is not constant, but rather is a variable that ranges from 0.02 at medium-weight cruise conditions, to a maximum of 0.20 at light-weight descent conditions. (You may ignore heavy-weight take-off conditions for the purposes of this problem.)
   (a) Sketch the root locus as a function of the loop gain $K_1 K_2$.
   (b) Determine the gain K_2 necessary to yield roots with $\zeta = 0.7071$ with $K_1 = 0.02$ (medium-weight cruise conditions).
   (c) Using the value of K_2 you found in part (b), determine the ζ of the complex conjugate roots associated with the aircraft dynamics, assuming the system is in the light-weight descent mode.



Code Number_____

Problem 21 (ECE Upper Level)

Consider a message signal $m(t)$ with the spectrum $M(f)$ shown below. The message bandwidth $W = 2\ KHz$. A DSB-LC (AM-modulated) signal, $s(t)$ is produced by modulating a carrier with $m(t)$.



(a) Sketch the spectrum of $s(t)$ when the carrier frequency $f_c = 4\ KHz$. Clearly label all frequencies.

(b) What is the lowest carrier frequency for which there is no sideband overlap.

Code Number_____

Problem 22 (ECE Upper Level)

A lossless 10 – turn helical antenna with a circumference of one –wavelength is connected to a 78-ohm coaxial line, and it is used as a transmitting antenna in a 500 MHz spacecraft communication system. The spacing between turns is $\lambda/10$. The power in the coaxial line from the transmitter is 5 watts. Assuming the antenna is lossless:

a. What is the radiated power?
b. If the antenna were isotropic, what would the power density (watts/m^2) be at a distance of 10 kilometers?
c. What is the power density (watts/m^2) at the same distance when the transmitting antenna is the 10-turn helix and the observations are made along the maximum of the major lobe?
d. If at 10 kilometers along the maximum of the major lobe an identical 10-turn helix was placed as a receiving antenna, which was polarization-matched to the incoming wave, what is the maximum power (in watts) that can be received?

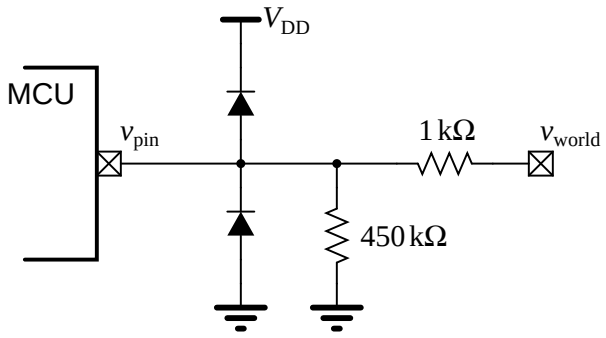
Code Number _____

Problem 23 (ECE Upper Level)

How *low* can the voltage v_{world} be driven by a careless student before a diode current exceeds 100 mA? What is the voltage at the MCU input pin? Assume that $V_{\text{DD}} = 5\,\text{V}$.

Table 1: $I - V$ data for the 1N4148 diode (a high conductance, fast diode)

V_{diode}	I_{diode}		V_{diode}	I_{diode}		V_{diode}	I_{diode}		V_{diode}	I_{diode}
-100 V	-100 nA		0 V	0 A		550 mV	$250\,\mu$A		900 mV	100 mA
-70 V	-40 nA		275 mV	$1\,\mu$A		600 mV	$700\,\mu$A		1.0 V	180 mA
-50 V	-25 nA		300 mV	$2\,\mu$A		650 mV	2 mA		1.1 V	270 mA
-30 V	-20 nA		350 mV	$5\,\mu$A		700 mV	5 mA		1.2 V	380 mA
-20 V	-17 nA		400 mV	$15\,\mu$A		750 mV	10 mA		1.3 V	525 mA
-10 V	-15 nA		450 mV	$35\,\mu$A		800 mV	20 mA		1.4 V	700 mA
-5 V	-15 nA		500 mV	$100\,\mu$A		850 mV	60 mA		1.45 V	850 mA



(Your analysis process is more important than the actual number, so clearly show how you arrive at your answer)

Code Number _____

Problem 23 (ECE Upper Level)

(CONTINUED)

Code Number _____

Problem 24 (ECE Upper Level)

Explain the basic idea how a receiver in a computer network detects errors in the received frame and how the errors can be corrected in ARQ protocols.

Code Number_____

Problem 25 (ECE Upper Level)

Modern operating systems provide a virtual memory service to executing processes. Explain the following concepts regarding virtual memory.

1. What is virtual memory, why is it needed, and how is it different from physical (real) memory?

2. Explain how the memory management unit in the processor implements virtual memory using pages (hint: explain the structure and semantics of the page table and page table entries).

3. Explain the role of the OS in virtual memory management (hint: explain how the OS performs memory allocation and page replacement).